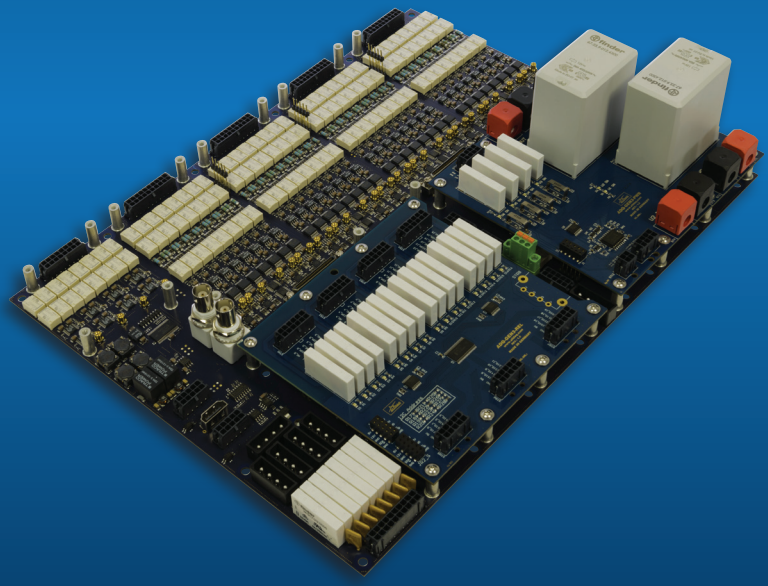
ALLDAQ

Competence in Measurement

ADQ-SCU

Manual

Rev. 1.01 EN



ALLDAQ Signal Condition Unit including Base Board, Power Board and Relay Board

Imprint

Manual ADQ-SCU
Rev. 1.01 EN
Date: 04/20/2018

Manufacturer and Support

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All information contained in this manual has been reviewed with great care. Nevertheless errors cannot be eliminated completely. Specifications and the content of this manual are subject to change without notice.

We are appreciated for notification of possible errors.

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Table of Content

1. Introduction

Please check the box and the content for damages and completeness before taking the device into operation. If any fault should be detected please inform us immediately.

- Shows the packing some evidence to damaging during transport?
- Any traces of use to be recognized at the device?

The device may not be taken into operation if it is damaged. In case of doubt please contact our technical service department.

Please read – before installing and programming the device – this manual watchfully!

1.1 Scope of delivery

- ALLDAQ base board ADQ-SCU-BB for signal condition unit
- Mezzanine board ALLDAQ power board ADQ-SCU-PB
- Mezzanine board ALLDAQ relay board ADQ-SCU-RB

Optional:

- 2 x 68-pin VHDCI cable (male - male), double-shielded, twisted-pair wires, length: 1.2 m (ADQ-CR-VHDCI-68M/68M-1,2m), art. no.: 150597 (2 x)
- 2 x 68-pin VHDCI cable (male - male), double-shielded, twisted-pair wires, length: 1.8 m (ADQ-CR-VHDCI-68M/68M-1,8m), art. no.: 146813 (2 x)
- HDMI cable, length: 1 m (ADQ-CR-HDMI-MM-1m), art. no.: 127015

1.2 Safety instructions

Necessarily note the following advices:

- Necessarily avoid touching of cables and connectors.
- Never expose the device to direct solar radiation during operation.
- Never run the device near heat sources.
- Protect the device before humidity, dust, liquids and fumes.
- Don´t use the device in damp rooms and never in explosive areas.
- A repair may only be done by trained and authorized persons.

- Please note before initial operation of the device especially when using voltages greater 42 V the installation rules and all relevant standards (including VDE standards).
- We recommend to tie all unused inputs basically to the corresponding reference ground to avoid cross talk between the input lines.

- Before connecting or removing cables with your signal condition unit (ADQ-SCU including mezzanine boards) from the power supply always disconnect your field wiring of the analog and digital I/Os and the connection to the ADQ-344.

- Ensure that no static discharge can occur passing the board when handling it. Follow the standard ESD safety precautions.
- Never connect devices with voltage-carrying parts, especially not with mains voltage.
- The user must take appropriate precautions to avoid unforseeable misuse.

For damages caused by improper use and subsequent damages any liability by ALLNET® GmbH Computersysteme is excluded.

1.3 Location of installation and mounting

The signal condition unit (ADQ-SCU including mezzanine boards) is for installation into measurement and test systems by specialised staff. All relevant installation instructions and standards must be followed.

The ADQ-SCU may only be used in dry rooms. Ensure a very good ventilation. Take care for proper fitting of the connection cables. Installation has to be done in a way that the cables are not in tension else they could release itself.

1.4 Short description

The ADQ-SCU signal condition unit was developed to optimally adapt a large number of analog and digital inputs/outputs to the requirements of a complex, automated test system. The signals are acquired and generated synchronously via the ADQ-344 multi-function measurement and control board, which also controls the ADQ-SCU via I^2C bus.

- Audio signal analysis of various levels
- Individual settings of input coupling (AC/DC), digital filters, gain and attenuation
- Measurement and mathematical evaluation of crucial values
- Monitoring stage for access to all audio channels
- Generation of audio signals for stimulation of power amplifiers
- Operating power switched by relays
- Currents up to 100 A (12 VDC) switched by relays
- Customer-specific extensions via mezzanine boards
- Easy control via I^2C bus
- Programming interface (API) for easy integration into your application
- Optimized for operation with the isolated data-acquisition and control board ADQ-344

2. The system in overview

2.1 Block diagram

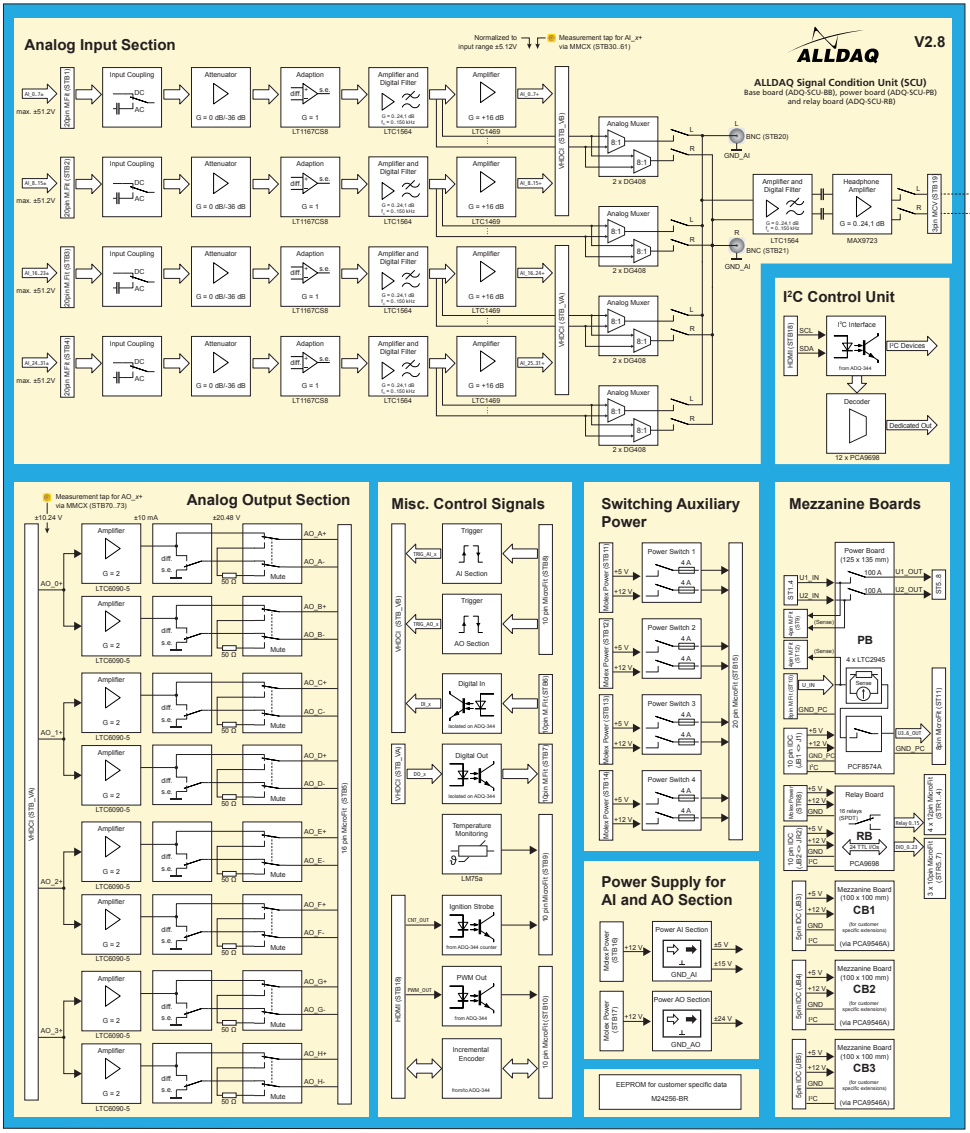


Figure 1: Block diagram ADQ-SCU

2.2 Base board ADQ-SCU-BB

Base board for signal condition unit (SCU) for connection with ADQ-344.

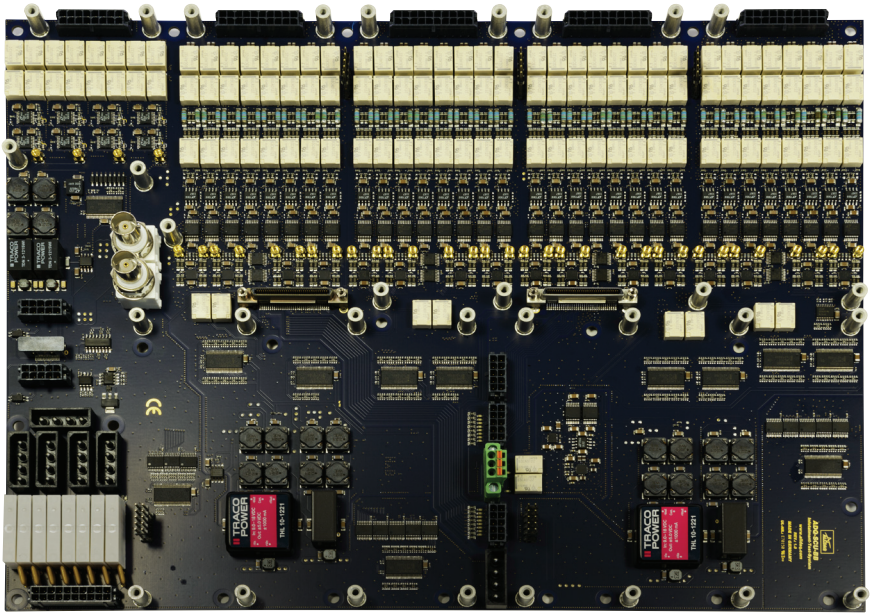


Figure 2: Base board ADQ-SCU-BB

AI section

- 32 differential analog inputs, input range programmable per channel (max. ±51.2 V)
- AC/DC coupling progammable per channel
- -36 dB attenuation stage can be enabled per channel
- Digital filter stage programmable per channel (cut-off frequency can be set from 0 to 150 kHz in steps of 10 kHz)
- Programmable gain per channel (factor: 1..16, this equals: 0..24.1 dB)
- Monitoring stage: stereo headphone amplifier for direct connection of a headphone
- 4 digital trigger inputs

AO section

- 4/8 analog outputs, output range ±20.48 V / max. 10 mA
- Switching between reference to ground and common mode output per channel
- Mute function
- 4 digital trigger inputs

More features

- Temperature monitoring of the base board with threshold value setting and an opto-isolated alarm output
- 3 places for customer-specific mezzanine boards
- PWM output (opto-isolated)
- Input for the ignition signal "Clamp 15" (opto-isolated)
- 8 isolated digital inputs
- 8 isolated digital outputs
- Complete control via I^2C bus
- Power lines switchable via relays (4 x +5V/4A; 4 x +12V/4A)
- Power supply by a PC power supply (+5V, +12V)

2.3 Power board ADQ-SCU-PB

Power board for signal condition unit (SCU) to be plugged onto the ADQ-SCU-BB.

Note: Boards of the initial series (Rev. 1.0) are labeled with ADQ-GEN3-PWR.

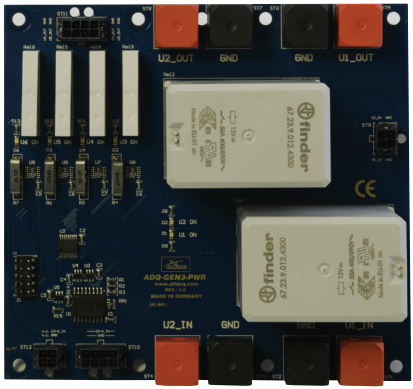


Abb. 3: Powerboard ADQ-SCU-PB

- Power mezzanine board (I^2C controlled)
- 2 x high current relays up to 12 VDC/100 A max. per relay (sense line at the relay input)
- 4 x power (U3..6) switchable via relays up to 30 VDC/5 A max. per relay (sense line at the relay input)
- 4-channel powermeter for U3..6

2.4 Relay board ADQ-SCU-RB

Relay board for signal condition unit (SCU) to be plugged onto the ADQ-SCU-BB.

Note: Boards of the initial series (Rev. 1.0) are labeled with ADQ-GEN3-REL.

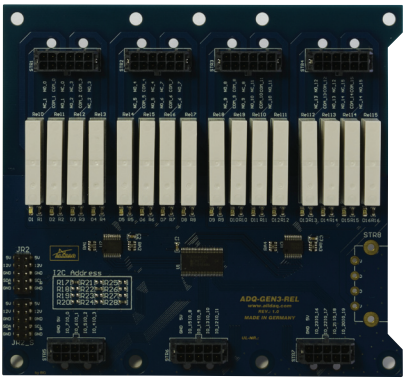


Figure 4: Relay board ADQ-SCU-RB

- Relay mezzanine board (I^2C controlled)
- 16 SPDT relays (form C), 30 VDC/6 A max.
- 24 TTL-I/Os (source: 10 mA max., sink: 25 mA max.)

2.5 Multi-function board ADQ-344

The signal condition unit ADQ-SCU was developed for connection to the multi-functional data-acquisition and control board ALLDAQ ADQ-344, which also handles controlling the ADQ-SCU by I^2C bus. The connection is established by two 68-pin VHDCI cables and one HDMI cable for miscellaneous special functions like the I^2C bus controlling the ADQ-SCU.

The ADQ-344 provide the following basic functions:

- 32 pseudo differential 18 bit voltage inputs up to 800 kS/s
- Input ranges: ±10.24 V, ±5.12 V, 0-10.24 V, 0-5.12 V
- Isolation voltage AI section: 1500 VDC (60 s)
- Four 16 bit voltage outputs (±10.24 V) up to 500 kS/s
- Isolation voltage AO section: 1500 VDC (60 s)
- 16 TTL-DIOs (3.3 V/5 V), 20 mA max. per output
- 8 isolated digital inputs (High: 15..35 V)
- 8 isolated digital outputs up to 600 mA per output
- Isolation voltage DI and DO section: 500 VAC
- Special functions via HDMI connector: 32 bit counter, I^2C bus port, incremental encoder port, frequency measurement, PWM output

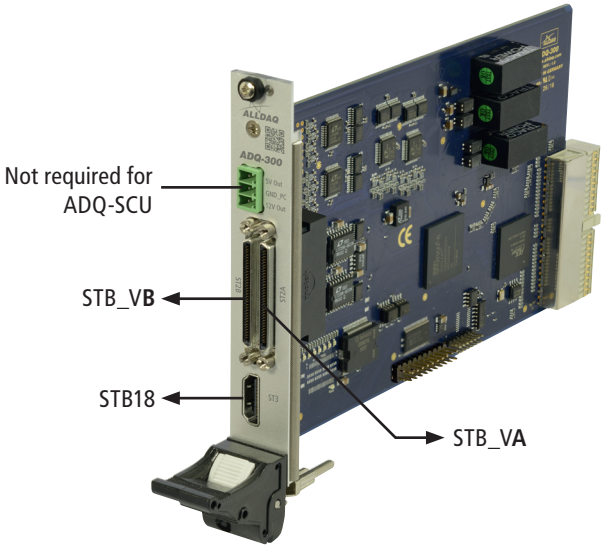


Figure 5: Multi-function board ADQ-344

2.6 Example system configuration

Typical configuration with an ADQ-Express measurement system, equipped with 2 multi-function boards of type ADQ-344 for controlling one signal condition unit ADQ-SCU each. Furthermore for each DUT one current measurement channel of the ADQ-412 will be connected with a power board ADQ-SCU-PB.

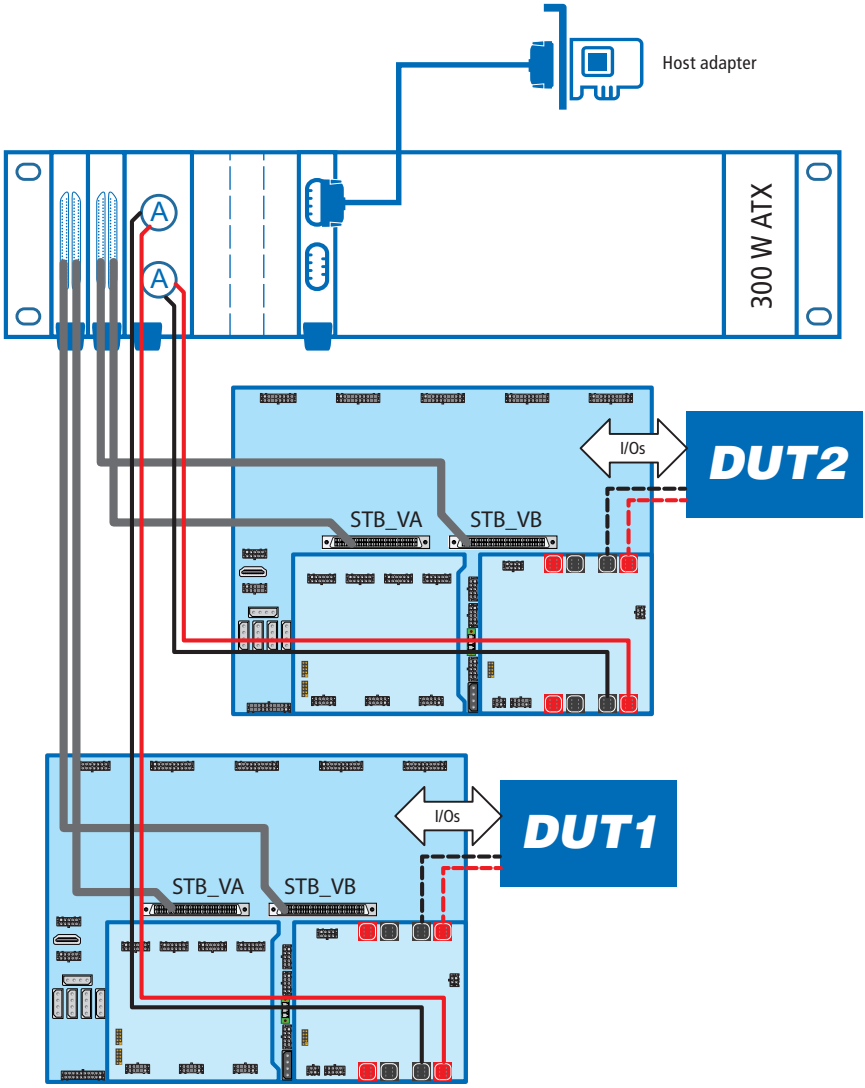


Figure 6: Example system configuration

3. Pin assignments

3.1 Position of the connectors

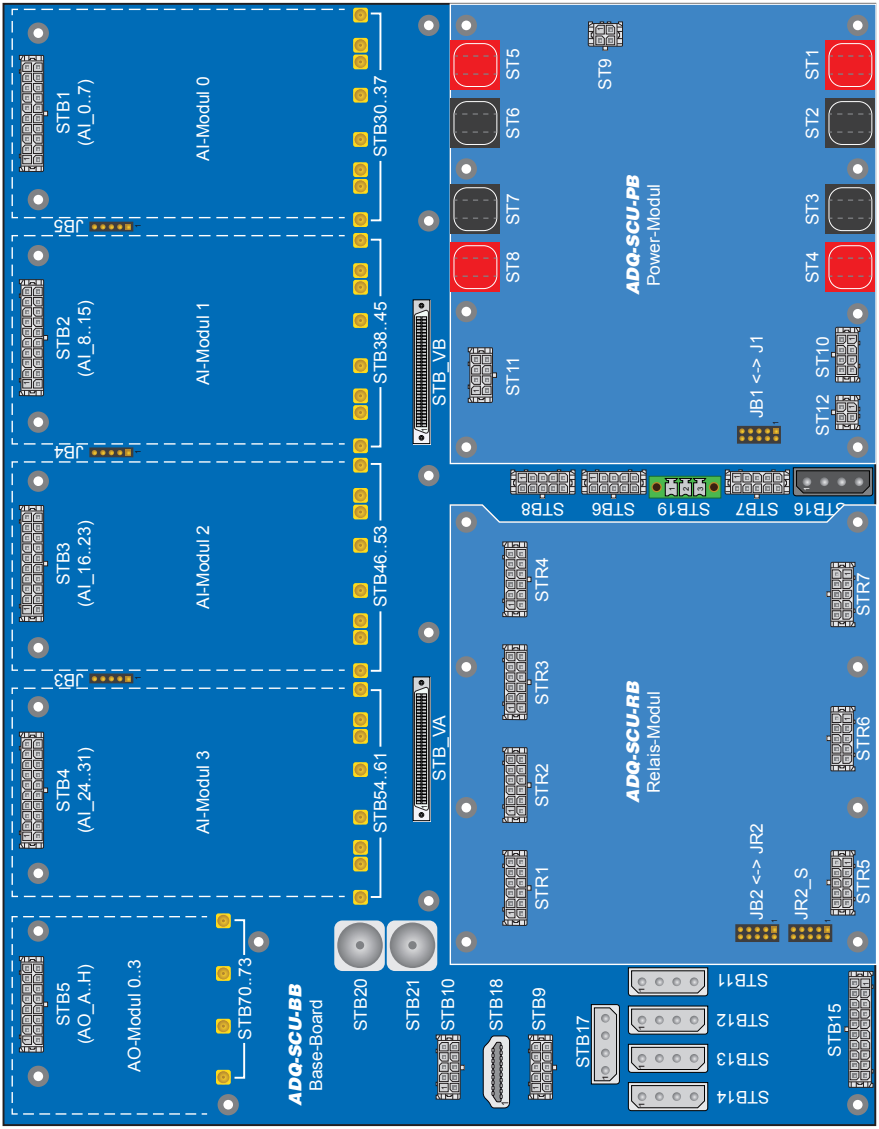


Figure 7: Position of the connectors

3.2 Prefixes of the connector names

STB: Connectors on the base board (ADQ-SCU-BB)

ST: Connectors on the power board (ADQ-SCU-PB)

STR: Connectors on the relay board (ADQ-SCU-RB)

J*x*: IDC connectors for connection from base board to the mezzanine boards

3.3 Connector types in overview

3.3.1 Type Molex

There are many connectors of the Molex 8981 series in use as well as double-row Micro-Fit connectors of the Molex 43045 series with 0.762 µm gold plating in different pin numbers.

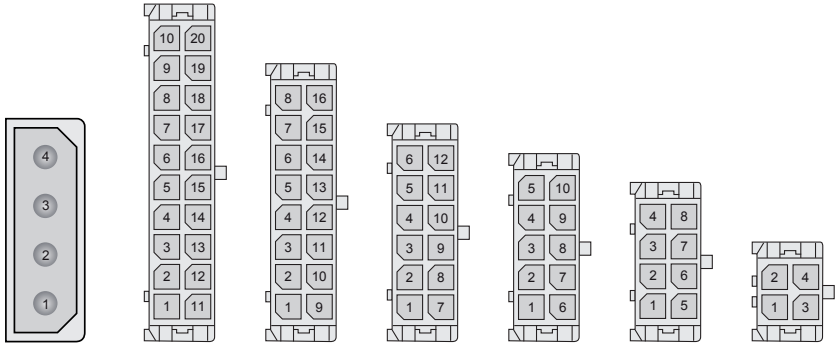


Figure 8: Molex connectors (top view)

3.3.2 Type IDC connectors

For connection between base board and mezzanine boards 10 and 5-pin IDC connectors are used (pitch: 2.54 mm).

Figure 9: IDC connector (top view)

3.3.3 Type Phoenix MCV

Figure 10: 3-pin headphone connector (top view)

Connector type: 3-pin header, Phoenix MCV 1,5/ 3-GF-3,5; order no.: 1843237

Mating plug with push-in spring connection: Phoenix FMC 1,5/ 3-STF-3,5; order no.: 1966101

3.3.4 Receptables for Micro-Fit connectors

We recommend the receptacle housings of the series 43025-*xy*10 with UL 94V-2 approval.

Circuits	Header type on ADQ-SCU	Receptable housing	Quantity BB/PB/RB	Quantity total
4-pin	43045-0426	43025-0410	0 / 2 / 0	2
8-pin	43045-0826	43025-0810	0 / 2 / 0	2
10-pin	43045-1026	43025-1010	5 / 0 / 3	8
12-pin	43045-1226	43025-1210	0 / 0 / 4	4
16-pin	43045-1626	43025-1610	1 / 0 / 0	1
20-pin	43045-2026	43025-2010	5 / 0 / 0	5

Table 1: Overview receptables

For all receptables in the table above 268 female crimp terminals are required in total. Depending on your requirements the following options are possible:

We recommend to use gold-plated contacts.

Current per contact	AWG	Material	Contact	Type
0.36 A - 0.14 A	26-30 AWG (0.13 - 0.05 mm^2)	Phosphor Bronze	tin-plated	43030-0010
0,36 A - 0.14 A	26-30 AWG (0.13 - 0.05 mm^2)	Phosphor Bronze	**gold-plated**	43030-0011
1.5 A - 0.6 A	20-24 AWG (0.52 - 0.21 mm^2)	Phosphor Bronze	tin-plated	43030-0007
1.5 A - 0.6 A	20-24 AWG (0.52 - 0.21 mm^2)	Phosphor Bronze	**gold-plated**	43030-0008
2.3 A	18 AWG (0.75 mm^2)	Phosphor Bronze	tin-plated	43030-0038

Table 2: Overview female crimp terminals

Attention!

Please follow the notes from Molex for an expert crimping of the Micro-Fit connectors!

3.4 Base board (ADQ-SCU-BB)

3.4.1 Analog input section (STB1..4)

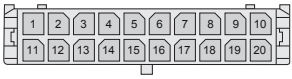


Figure 11: 20-pin Micro-Fit 43045-2026

The corresponding MMCX coaxial connectors (STB30..61) are indicated in brackets. They can be used as measurement taps for the analog input signals which are forwarded to the ADQ-344.

Pin	STB1 (Module 0)	STB2 (Module 1)	STB3 (Module 2)	STB4 (Module 3)
1	GND_AI	GND_AI	GND_AI	GND_AI
2	AI_0+ (STB30)	AI_8+ (STB38)	AI_16+ (STB46)	AI_24+ (STB54)
3	AI_1+ (STB31)	AI_9+ (STB39)	AI_17+ (STB47)	AI_25+ (STB55)
4	AI_2+ (STB32)	AI_10+ (STB40)	AI_18+ (STB48)	AI_26+ (STB56)
5	AI_3+ (STB33)	AI_11+ (STB41)	AI_19+ (STB49)	AI_27+ (STB57)
6	AI_4+ (STB34)	AI_12+ (STB42)	AI_20+ (STB50)	AI_28+ (STB58)
7	AI_5+ (STB35)	AI_13+ (STB43)	AI_21+ (STB51)	AI_29+ (STB59)
8	AI_6+ (STB36)	AI_14+ (STB44)	AI_22+ (STB52)	AI_30+ (STB60)
9	AI_7+ (STB37)	AI_15+ (STB45)	AI_23+ (STB53)	AI_31+ (STB61)
10	GND_AI	GND_AI	GND_AI	GND_AI
11	GND_AI	GND_AI	GND_AI	GND_AI
12	AI_0- (STB30)	AI_8- (STB38)	AI_16- (STB46)	AI_24- (STB54)
13	AI_1- (STB31)	AI_9- (STB39)	AI_17- (STB47)	AI_25- (STB55)
14	AI_2- (STB32)	AI_10- (STB40)	AI_18- (STB48)	AI_26- (STB56)
15	AI_3- (STB33)	AI_11- (STB41)	AI_19- (STB49)	AI_27- (STB57)
16	AI_4- (STB34)	AI_12- (STB42)	AI_20- (STB50)	AI_28- (STB58)
17	AI_5- (STB35)	AI_13- (STB43)	AI_21- (STB51)	AI_29- (STB59)
18	AI_6- (STB36)	AI_14- (STB44)	AI_22- (STB52)	AI_30- (STB60)
19	AI_7- (STB37)	AI_15- (STB45)	AI_23- (STB53)	AI_31- (STB61)
20	GND_AI	GND_AI	GND_AI	GND_AI

Table 3: Pin assignment STB1..4

AI modulee 0	AI_0 (STB30)… AI_7 (STB37)
AI modulee 1	AI_8 (STB38)… AI_15 (STB45)
AI modulee 2	AI_16 (STB46)…AI_23 (STB53)
AI modulee 3	AI_24 (STB54)…AI_31 (STB61)

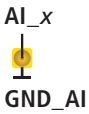


Figure 12: MMCX connectors STB30..61

3.4.2 Analog output section (STB5)

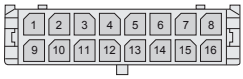


Figure 13: 16-pin Micro-Fit 43045-1626

Pin	STB5	Comment
1	AO_A+	Corresponding output signal from AO_0+
2	AO_B+	Corresponding output signal from AO_0+
3	AO_C+	Corresponding output signal from AO_1+
4	AO_D+	Corresponding output signal from AO_1+
5	AO_E+	Corresponding output signal from AO_2+
6	AO_F+	Corresponding output signal from AO_2+
7	AO_G+	Corresponding output signal from AO_3+
8	AO_H+	Corresponding output signal from AO_3+
9	AO_A–	Alternatively common phase with AO_A+ or reference to GND_AO
10	AO_B–	Alternatively common phase with AO_B+ or reference to GND_AO
11	AO_C–	Alternatively common phase with AO_C+ or reference to GND_AO
12	AO_D–	Alternatively common phase with AO_D+ or reference to GND_AO
13	AO_E–	Alternatively common phase with AO_E+ or reference to GND_AO
14	AO_F–	Alternatively common phase with AO_F+ or reference to GND_AO
15	AO_G–	Alternatively common phase with AO_G+ or reference to GND_AO
16	AO_H–	Alternatively common phase with AO_H+ or reference to GND_AO

Table 4: Pin assignment STB5

The corresponding MMCX coaxial connectors (STB70..73) which can be used as measurement taps for the analog output signals from the ADQ-344.

AO modulee 0	AO_0+ from ADQ-344 (STB70)
AO modulee 1	AO_1+ from ADQ-344 (STB71)
AO modulee 2	AO_2+ from ADQ-344 (STB72)
AO modulee 3	AO_3+ from ADQ-344 (STB73)

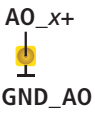


Figure 14: MMCX connectors STB70..73

3.4.3 Digital-I/O section (STB6..7)

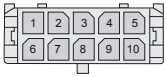


Figure 15: 10-pin Micro-Fit 43045-1026

Pin	STB6 (DI)	STB7 (DO)
1	GND_DI	DO_0
2	DI_0	DO_2
3	DI_2	DO_4
4	DI_4	DO_6
5	DI_6	V_EXT_DO
6	V_EXT_DI	DO_1
7	DI_1	DO_3
8	DI_3	DO_5
9	DI_5	DO_7
10	DI_7	GND_DO

Table 5: Pin assignment STB6..7

3.4.4 External trigger inputs for AI/AO section (STB8)

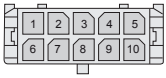


Figure 16: 10-pin Micro-Fit 43045-1026

Pin	STB8	Comment
1	TRIG_AO_0	Trigger input for analog output module AO_0 of the ADQ-344 (= AO_A/B)
2	TRIG_AO_2	Trigger input for analog output module AO_2 of the ADQ-344 (= AO_E/F)
3	TRIG_AO_GND	Reference ground for trigger of analog outputs
4	TRIG_AI_2	Trigger input for analog input module 2 of the ADQ-344 (= AI_16..23)
5	TRIG_AI_0	Trigger input for analog input module 0 of the ADQ-344 (= AI_0..7)
6	TRIG_AO_1	Trigger input for analog output module AO_1 of the ADQ-344 (= AO_C/D)
7	TRIG_AO_3	Trigger input for analog output module AO_3 of the ADQ-344 (= AO_G/H)
8	TRIG_AI_GND	Reference ground for trigger of analog inputs
9	TRIG_AI_3	Trigger input for analog input module 3 of the ADQ-344 (= AI_24..31)
10	TRIG_AI_1	Trigger input for analog input module 1 of the ADQ-344 (= AI_8..15)

Table 6: Pin assignment STB8

3.4.5 Counter, ignition signal & temperature alarm (STB9)

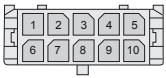


Figure 17: 10-pin Micro-Fit 43045-1026

Pin	STB9	Comment
1	TEMP_OUT	Open collector output of temperature monitoring on the base board (V_{CE} = 50 V / $I_{max.}$ = 250 mA)
2	IGN_STROBE	Opto-isolated input for ignition signal ("Clamp 15")
3	CNT_EXT_CLK	External clock input for counter
4	CNT_EN	External enable input for counter
5	CNT_TRIG	External trigger input for counter
6	VCC_PC	+5 V from PC
7	GND_PC	PC ground
8	GND_PC	PC ground
9	GND_PC	PC ground
10	GND_PC	PC ground

Table 7: Pin assignment STB9

3.4.6 Special functions (STB10)

This connector combines the signals for frequency measurement, PWM output and the incremental encoder.

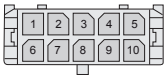


Figure 18: 10-pin Micro-Fit 43045-1026

Pin	STB10	Comment
1	GND_PC	PC ground
2	GND_PC	PC ground
3	PWM_EN	Enable input for PWM output
4	GND_PC	PC ground
5	INC_A	Incremental encoder input (channel A)
6	FRQ_IN	Input for frequency measurement
7	PWM_OUT	Opto-isolated output for rectangular signal with adjustable duty factor
8	GND_PC	PC ground
9	INC_B	Incremental encoder input (channel B)
10	INC_EXT_RST	Incremental encoder reset input

Table 8: Pin assignment STB10

3.4.7 Switchable auxiliary power (STB11..14, STB15)

Power input from PC power supply via four Molex connectors (STB11..14). The voltages +12 V (12V_IN_1..4) and +5 V (5V_IN_1..4) are applied seperately and output via relay at STB15.

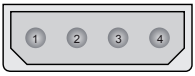


Figure 19: 4 x 4-pin Molex 8981 series (180°), (STB11..14)

Pin	STB11 (Switch 1)	STB12 (Switch 2)	STB13 (Switch 3)	STB14 (Switch 4)
1	12V_IN_1	12V_IN_2	12V_IN_3	12V_IN_4
2	GND_PC	GND_PC	GND_PC	GND_PC
3	GND_PC	GND_PC	GND_PC	GND_PC
4	5V_IN_1	5V_IN_2	5V_IN_3	5V_IN_4

Table 9: Pin assignment STB11..14

Power outputs (4 x +5 V / 4 A, 4 x +12 V / 4 A) at STB15 switchable by relays. Each output is protected by a 4 A fuse of type Polyfuse.

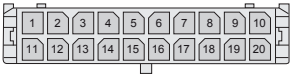


Figure 20: 1 x 20-pin Micro-Fit 43045-2026 (STB15)

Pin	STB15	Comment
1	GND_PC	PC ground
2	GND_PC	PC ground
3	GND_PC	PC ground
4	GND_PC	PC ground
5	GND_PC	PC ground
6	GND_PC	PC ground
7	GND_PC	PC ground
8	GND_PC	PC ground
9	GND_PC	PC ground
10	GND_PC	PC ground
11	12V_OUT_1	Output of switchable 12 V power line (4 A)
12	5V_OUT_1	Output of switchable 5 V power line (4 A)
13	12V_OUT_2	Output of switchable 12 V power line (4 A)
14	5V_OUT_2	Output of switchable 5 V power line (4 A)
15	GND_PC	PC ground
16	GND_PC	PC ground
17	12V_OUT_3	Output of switchable 12 V power line (4 A)
18	5V_OUT_3	Output of switchable 5 V power line (4 A)
19	12V_OUT_4	Output of switchable 12 V power line (4 A)
20	5V_OUT_4	Output of switchable 5 V power line (4 A)

Table 10: Pin assignment STB15

3.4.8 Power supply for base board (STB16..17)

Power lines from PC power supply via two Molex connectors (STB16..17) for supply of base board, power board and relay board with ±5 V, ±15 V and ±24 V.

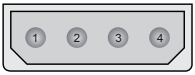


Figure 21: 2 x 4-pin Molex, 8981 series (180°), (STB16..17)

Pin	STB16	STB17
1	12V_IN (+12 V PC)	12V_IN (+12 V PC)
2	GND_PC	GND_PC
3	GND_PC	GND_PC
4	5V_IN (+5V PC)	5V_IN (+5V PC)

Table 11: Pin assignment STB16..17

3.4.9 HDMI connector for special functions (STB18)

HDMI connector for linking the following special functions of the ADQ-344 to the base board:

- 32 bit counter (prefix: CNT…)
- I^2C bus port (prefix: I2C…)
- Incremental encoder port (prefix: INC…)
- Frequency measurement input (prefix: FRQ…)
- PWM output (prefix: PWM…)

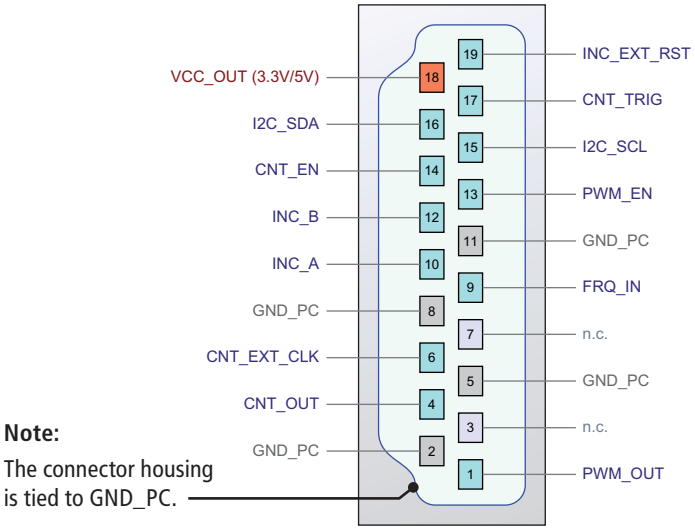


Figure 22: HDMI connector (STB18)

Pin	STB18	Comment
1	PWM_OUT	Input for PWM output from the ADQ-344
2	GND_PC	PC ground
3	n.c.	reserved
4	CNT_OUT	Input for strobe output of the counter from the ADQ-344
5	GND_PC	PC ground
6	CNT_EXT_CLK	Output to the external clock input for counter of the ADQ-344
7	n.c.	reserved
8	GND_PC	PC ground
9	FRQ_IN	Output to frequency measurement input of the ADQ-344
10	INC_A	Output to incremental encoder input (channel A) of the ADQ-344
11	GND_PC	PC ground
12	INC_B	Output to incremental encoder input (channel B) of the ADQ-344
13	PWM_EN	Output to enable input for PWM output of the ADQ-344
14	CNT_EN	Output to enable input for counter of the ADQ-344
15	I2C_SCL	Clock input for I^2C bus of the ADQ-344
16	I2C_SDA	Data input for I^2C bus of the ADQ-344
17	CNT_TRIG	Output to external trigger input for counter of the ADQ-344
18	VCC_IN_344	3.3 V/5 V power supply from the ADQ-344
19	INC_EXT_RST	Output to incremental encoder reset input of the ADQ-344

Table 12: Pin assignment STB18

3.4.10 Audio output (STB19)

Stereo audio output for connection of a headphone. The output can be switched by relay, which gives you the possibility to wire the audio outputs of several base boards in parallel.

Attention:

In case of parallel connection of audio outputs of several base boards, you must ensure that never two or more outputs are active at the same time (relay closed). Otherwise the output stage may be damaged.

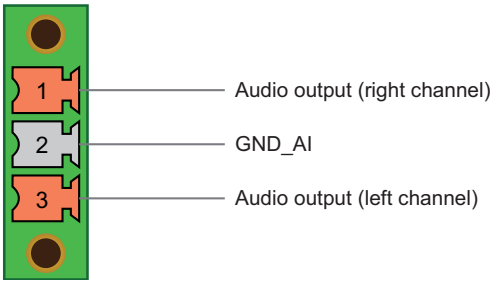


Figure 23: Audio output (STB19)

Connector type: 3-pin header, Phoenix MCV 1,5/ 3-GF-3,5; order no.: 1843237

Mating plug with push-in spring connection: Phoenix FMC 1,5/ 3-STF-3,5; order no.: 1966101

3.4.11 Measurement signal tap (STB20..21)

Measurement signal tap between digital filter stage and output amplifier. By appropriate control of the analog multiplexer stage and the following relays each of the 32 AI channels can be routed to any of the both BNC female connectors.

Note:

Only switch one AI channel to a certain BNC connector at the same time!

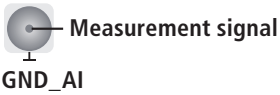


Figure 24: 2 x BNC female connector (STB20..21)

3.4.12 68-pin VHDCI female connectors from/to ADQ-34x (STB_VA/B)

The following pin assignment refers to the VHDCI female connectors at the ADQ-344. I. e. the direction of the signals on base board side has to be considered reverse.

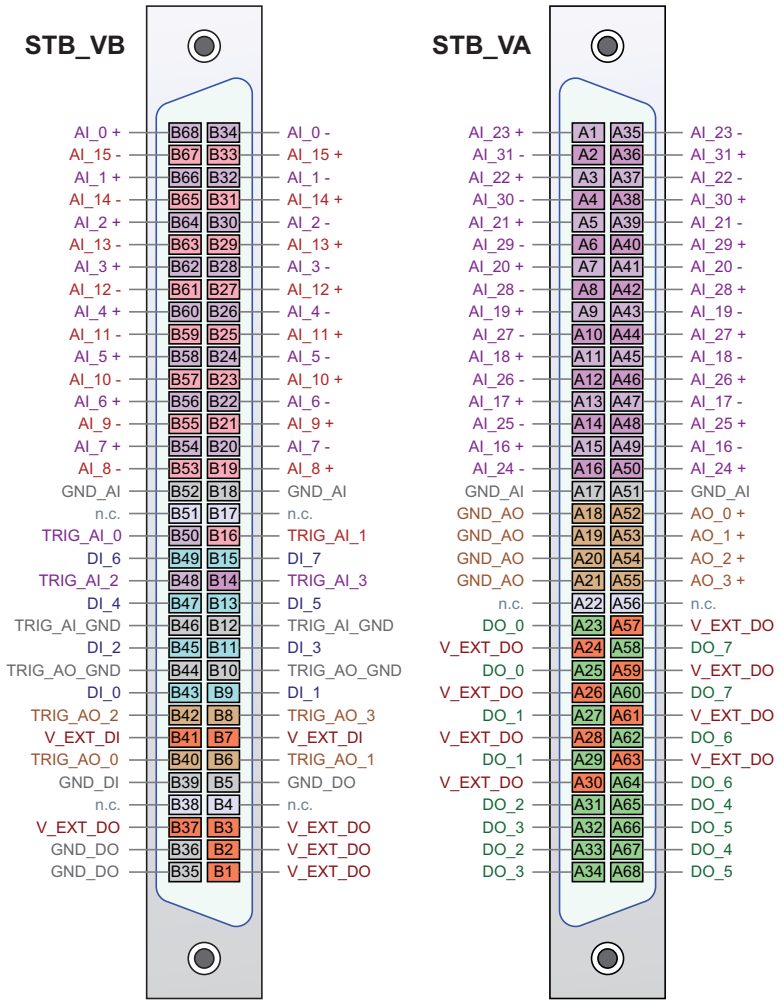


Figure 25: Pin assignment STB_VA and STB_VB

3.5 Power board (ADQ-SCU-PB)

3.5.1 IDC connector JB1 -> J1

By the double-row IDC connector JB1 -> J1 the power board is connected to the base board.

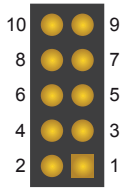


Figure 26: 10-pin IDC connector (JB1 / J1)

Pin	Comment	Pin	Comment
1	GND_PC	2	GND_PC
3	SCL_BASE	4	SDA_BASE
5	GND_PC	6	GND_PC
7	+12 V PC	8	+12 V PC
9	+5 V PC	10	+5 V PC

Table 13: Pin assignment JB1/J1

3.5.2 High current supply schaltbar (ST1..8)

By ST1..8 two power supplies with 100 A/12 V maximum per channel can be switched via relays.

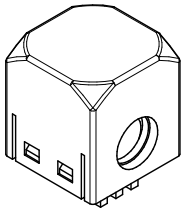


Figure 27: 8 x single-pole high current connector of type:
Würth Electronic REDCUBE Direct Plug Terminal WP-PLUG.

ST..		Comment
ST1	U1_IN	Input $U1_{IN}$
ST2	GND_PC	PC ground
ST3	GND_PC	PC ground
ST4	U2_IN	Input $U2_{IN}$
ST5	U1_OUT	Relay output $U1_{OUT}$
ST6	GND_PC	PC ground
ST7	GND_PC	PC ground
ST8	U2_OUT	Relay output $U2_{OUT}$

Table 14: Pin assignment ST1..8

3.5.3 Sense connector (ST9)

Sense connector for monitoring the voltage at the inputs $U1_{IN}$ and $U2_{IN}$.

Figure 28: 4-pin Micro-Fit 43045-0426

Pin	ST9	Comment
1	GND_PC	PC ground
2	GND_PC	PC ground
3	U2_SENSE	Sense connector for $U2_{IN}$ (coming from ST4)
4	U1_SENSE	Sense connector for $U1_{IN}$ (coming from ST1)

Table 15: Pin assignment ST9

3.5.4 Power lines switchable (ST10, ST11)

By ST10 and ST11 four power lines (30 V/5 A max. per channel) can be switched via relays. Voltage and current (via 20 mΩ shunt) can be measured per channel. By the applied I^2C power meter of type LTC2945 beside voltage (up to 30 VDC) and current (up to 5 A) also the power can be read directly.

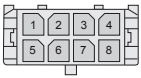


Figure 29: 8-pin Micro-Fit 43045-0826 (ST10, ST11)

Pin	ST10	ST11	Comment
1	GND_PC	GND_PC	PC ground
2	GND_PC	GND_PC	PC ground
3	GND_PC	GND_PC	PC ground
4	GND_PC	GND_PC	PC ground
5	U_IN	U6_OUT	Relay switches U_IN to U6
6	U_IN	U5_OUT	Relay switches U_IN to U5
7	U_IN	U4_OUT	Relay switches U_IN to U4
8	U_IN	U3_OUT	Relay switches U_IN to U3

Table 16: Pin assignment ST10, ST11

3.5.5 Sense connector (ST12)

Sense connector for monitoring the voltage U_IN (see ST10).

Figure 30: 4-pin Micro-Fit 43045-0426

Pin	ST12	Comment
1	GND_PC	PC ground
2	n.c.	not connected
3	U_SENSE	Sense connector for U_IN (coming from ST10)
4	n.c.	not connected

Table 17: Pin assignment ST12

3.6 Relayboard (ADQ-SCU-RB)

3.6.1 IDC connector JB2 -> JR2

By the double-row IDC connector JB2 -> JR2 the relay board is connected to the base board. 24 TTL-I/O channels (DIO_0..23) and 16 single-pole SPDT relays (type C) are available.

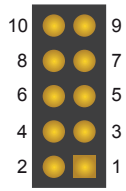


Figure 31: 10-pin IDC connector (JB2 / JR2)

Pin	Comment	Pin	Comment
1	GND_PC	2	GND_PC
3	SCL_BASE	4	SDA_BASE
5	GND_PC	6	GND_PC
7	+12 V PC	8	+12 V PC
9	+5 V PC	10	+5 V PC

Table 18: Pin assignment JB2/JR2

3.6.2 SPDT relays (STR1..4)

Pin assignment of the 16 SPDT relays. All switching contacts (NO/NC/COM) are routed to the connectors STR1..4. Load per relay (30 VDC/6 A max.).

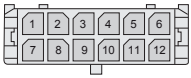


Figure 32: 4 x 12-pin Micro-Fit 43045-1226 (STR1..4)

Pin	STR1	STR2	STR3	STR4
1	NO_0 (Relay 0)	NO_4 (Relay 4)	NO_8 (Relay 8)	NO_12 (Relay 12)
2	COM_0 (Relay 0)	COM_4 (Relay 4)	COM_8 (Relay 8)	COM_12 (Relay 12)
3	NC_0 (Relay 0)	NC_4 (Relay 4)	NC_8 (Relay 8)	NC_12 (Relay 12)
4	NC_3 (Relay 3)	NC_7 (Relay 7)	NC_11 (Relay 11)	NC_15 (Relay 15)
5	COM_3 (Relay 3)	COM_7 (Relay 7)	COM_11 (Relay 11)	COM_15 (Relay 15)
6	NO_3 (Relay 3)	NO_7 (Relay 7)	NO_11 (Relay 11)	NO_15 (Relay 15)
7	NC_1 (Relay 1)	NC_5 (Relay 5)	NC_9 (Relay 9)	NC_13 (Relay 13)
8	COM_1 (Relay 1)	COM_5 (Relay 5)	COM_9 (Relay 9)	COM_13 (Relay 13)
9	NO_1 (Relay 1)	NO_5 (Relay 5)	NO_9 (Relay 9)	NO_13 (Relay 13)
10	NO_2 (Relay 2)	NO_6 (Relay 6)	NO_10 (Relay 10)	NO_14 (Relay 14)
11	COM_2 (Relay 2)	COM_6 (Relay 6)	COM_10 (Relay 10)	COM_14 (Relay 14)
12	NC_2 (Relay 2)	NC_6 (Relay 6)	NC_10 (Relay 10)	NC_14 (Relay 14)

Table 19: Pin assignment STR1..4

Note: Corresponding to the software the index of the relays starts with "0".

3.6.3 TTL Digital-I/Os (STR5..7)

At the connectors STR5..7 a total of 24 digital I/Os are provided, which can be switched by I^2C bus and the state can be read. The inputs and outputs are dimensioned for TTL level with a maximum load of 10 mA (source) and 25 mA (sink) per channel.

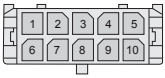


Figure 33: 3 x 10-pin Micro-Fit 43045-1026 (STR5..7)

Pin	STR5	STR6	STR7
1	DIO_4	DIO_12	DIO_20
2	DIO_5	DIO_13	DIO_21
3	DIO_6	DIO_14	DIO_22
4	DIO_7	DIO_15	DIO_23
5	GND_PC	GND_PC	GND_PC
6	DIO_3	DIO_11	DIO_19
7	DIO_2	DIO_10	DIO_18
8	DIO_1	DIO_9	DIO_17
9	DIO_0	DIO_8	DIO_16
10	+5V PC	+5V PC	+5V PC

Table 20: Pin assignment STR5..7

3.6.4 STR8 (not applicable)

Power input from PC power supply for relay board (+5 V / +12 V).

Connector type: 1 x 4-pin Molex, 8981 series (90°)

Pin	STR8
1	+12 V PC
2	GND_PC
3	GND_PC
4	+5 V PC

Table 21: Pin assignment STR8

3.7 Customer-specific mezzanine boards (CB1..3)

By the single-row IDC connector JB3..5 three customer-specific mezzanine boards (CB1..3) can be connected to the base board.

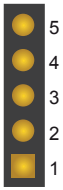


Figure 34: 3 x 5-pin IDC connector (JB3..5)

Pin	JB3 (CB1)	JB4 (CB2)	JB5 (CB3)
1	GND_PC	GND_PC	GND_PC
2	SCL_CB1	SCL_CB2	SCL_CB3
3	SDA_CB1	SDA_CB2	SDA_CB3
4	+12 V PC	+12 V PC	+12 V PC
5	+5 V PC	+5 V PC	+5 V PC

Table 22: Pin assignment JB3..5

4. I²C addresses

Note: The I²C addresses are given as a 7 bit value (slave address only) as well as an 8 bit value (slave address + read/write bit as LSB). The hexadecimal notation is marked by a trailing "h".

Via the I²C port of the ADQ-344 up to four data bytes can be sent in one transmission cycle.

4.1 Addresses in overview

Description	Chip	I²C address (7 bit/8 bit)
Base board ADQ-SCU-BB – AO section		
AO section disabling analog output at LTC6090-5	PCA9698	12h / 24h
Base board ADQ-SCU-BB – Control relays		
AO section s.e./diff switchover, mute, switchable power lines (switch 1..4)	PCA9698	13h / 26h
AI section (AI_0..15) AC/DC coupling, attenuation, relay monitoring stage	PCA9698	28h / 50h
AI section (AI_16..31) AC/DC coupling, attenuation, headphone output	PCA9698	29h / 52h
Base board ADQ-SCU-BB – Monitoring stage with headphone amplifier		
Stereo headphone amplifier with BassMax, volume control and I²C	MAX9723	4Ch / 98h
Base board ADQ-SCU-BB – AI module 0		
AI module 0 (AI_0..4), digital filter stage	PCA9698	22h / 44h
AI module 0 (AI_5..7), digital filter stage, monitoring stage filter (left/right)	PCA9698	23h / 46h
AI module 0, 8 channel analog multiplexer	PCF8574	20h / 40h
Base board ADQ-SCU-BB – AI module 1		
AI module 1 (AI_8..12), digital filter stage	PCA9698	24h / 48h
AI module 1 (AI_13..15), digital filter stage, 8 channel analog multiplexer	PCA9698	25h / 4Ah
Base board ADQ-SCU-BB – AI module 2		
AI module 2 (AI_16..20), digital filter stage	PCA9698	26h / 4Ch
AI module 2 (AI_21..23), digital filter stage, 8 channel analog multiplexer	PCA9698	27h / 4Eh
Base board ADQ-SCU-BB – AI module 3		
AI module 3 (AI_24..28), digital filter stage	PCA9698	10h / 20h
AI module 3 (AI_29..31), digital filter stage, 8 channel analog multiplexer	PCA9698	11h / 22h
Base board ADQ-SCU-BB – I²C switcher		
4 channel I²C master/slave switch	PCA9546A	70h / E0h
Base board ADQ-SCU-BB – I²C temperature monitoring		
I²C temperature monitoring with threshold setting and alarm output	LM75a	47h / 9Eh
Base board ADQ-SCU-BB – I²C EEPROM		
EEPROM for storage of user-specific data	M24256-BR	50h / A0h

Description	Chip	I²C address (7 bit/8 bit)
Relay board ADQ-SCU-RB – Relay mezzanine board		
Relay mezzanine board with 16 SPDT relays (form C), 24 TTL-I/Os	PCA9698	14h / 28h
Power board ADQ-SCU-PB – Power mezzanine board		
Relay control (U1..6): 2 high current relays, 4 standard relays	PCF8574A	39h / 72h
Power measurement (channel U3)	LTC2945	6Fh / DEh
Power measurement (channel U4)	LTC2945	6Ch/ D8h
Power measurement (channel U5)	LTC2945	67h / CEh
Power measurement (channel U6)	LTC2945	69h / D2h

4.2 Cut-off frequency and gain of LTC1564

The cut-off frequency is proportional to the binary value F3..0.

F3	F2	F1	F0	Cut-off frequency	G3	G2	G1	G0	Gain (voltage ratio)	Verstärkung (dB)
0	0	0	0	Mute	0	0	0	0	1	0
0	0	0	1	10 kHz	0	0	0	1	2	6.0
0	0	1	0	20 kHz	0	0	1	0	3	9.5
0	0	1	1	30 kHz	0	0	1	1	4	12.0
0	1	0	0	40 kHz	0	1	0	0	5	14.0
0	1	0	1	50 kHz	0	1	0	1	6	15.6
0	1	1	0	60 kHz	0	1	1	0	7	16.9
0	1	1	1	70 kHz	0	1	1	1	8	18.1
1	0	0	0	80 kHz	1	0	0	0	9	19.1
1	0	0	1	90 kHz	1	0	0	1	10	20.0
1	0	1	0	100 kHz	1	0	1	0	11	20.8
1	0	1	1	110 kHz	1	0	1	1	12	21.6
1	1	0	0	120 kHz	1	1	0	0	13	22.3
1	1	0	1	130 kHz	1	1	0	1	14	22.9
1	1	1	0	140 kHz	1	1	1	0	15	23.5
1	1	1	1	150 kHz	1	1	1	1	16	24.1

Table 23: Cut-off frequency and gain of LTC1564

4.3 Base board ADQ-SCU-BB

4.3.1 AI section (AI_0..15) AC/DC coupling, attenuation, relay monitoring stage

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	28h	50h	Control of port 0..5 with positive logic (via TBD62083A), outputs to be configured as source drivers; => Register 28h = 11h (default)

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	REL_CH7_ACDC_M0	AC/DC coupling AI_7+	Coupling: AC
PORT_IO0_1	REL_CH6_ACDC_M0	AC/DC coupling AI_6+	Coupling: AC
PORT_IO0_2	REL_CH5_ACDC_M0	AC/DC coupling AI_5+	Coupling: AC
PORT_IO0_3	REL_CH4_ACDC_M0	AC/DC coupling AI_4+	Coupling: AC
PORT_IO0_4	REL_CH3_ACDC_M0	AC/DC coupling AI_3+	Coupling: AC
PORT_IO0_5	REL_CH2_ACDC_M0	AC/DC coupling AI_2+	Coupling: AC
PORT_IO0_6	REL_CH1_ACDC_M0	AC/DC coupling AI_1+	Coupling: AC
PORT_IO0_7	REL_CH0_ACDC_M0	AC/DC coupling AI_0+	Coupling: AC
PORT_IO1_0	REL_7_M0	Attenuation AI_7+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_1	REL_6_M0	Attenuation AI_6+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_2	REL_5_M0	Attenuation AI_5+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_3	REL_4_M0	Attenuation AI_4+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_4	REL_3_M0	Attenuation AI_3+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_5	REL_2_M0	Attenuation AI_2+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_6	REL_1_M0	Attenuation AI_1+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_7	REL_0_M0	Attenuation AI_0+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO2_0	REL_CH0_ACDC_M1	AC/DC coupling AI_8+	Coupling: AC
PORT_IO2_1	REL_CH1_ACDC_M1	AC/DC coupling AI_9+	Coupling: AC
PORT_IO2_2	REL_CH2_ACDC_M1	AC/DC coupling AI_10+	Coupling: AC
PORT_IO2_3	REL_CH3_ACDC_M1	AC/DC coupling AI_11+	Coupling: AC
PORT_IO2_4	REL_CH4_ACDC_M1	AC/DC coupling AI_12+	Coupling: AC
PORT_IO2_5	REL_CH5_ACDC_M1	AC/DC coupling AI_13+	Coupling: AC
PORT_IO2_6	REL_CH6_ACDC_M1	AC/DC coupling AI_14+	Coupling: AC
PORT_IO2_7	REL_CH7_ACDC_M1	AC/DC coupling AI_15+	Coupling: AC

Port PCA9698	Signal in schematic	Description	Default
PORT_IO3_0	REL_0_M1	Attenuation AI_8+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_1	REL_1_M1	Attenuation AI_9+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_2	REL_2_M1	Attenuation AI_10+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_3	REL_3_M1	Attenuation AI_11+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_4	REL_4_M1	Attenuation AI_12+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_5	REL_5_M1	Attenuation AI_13+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_6	REL_6_M1	Attenuation AI_14+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_7	REL_7_M1	Attenuation AI_15+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO4_0	ABH_RE_M3	Monitoring relay for AI module 3 (AI_24..31) – right channel	OFF (no connection to monitor stage MAX9723)
PORT_IO4_1	ABH_LI_M3	Monitoring relay for AI module 3 (AI_24..31) – left channel	OFF (no connection to monitor stage MAX9723)
PORT_IO4_2	ABH_RE_M2	Monitoring relay for AI module 2 (AI_16..23) – right channel	OFF (no connection to monitor stage MAX9723)
PORT_IO4_3	ABH_LI_M2	Monitoring relay for AI module 2 (AI_16..23) – left channel	OFF (no connection to monitor stage MAX9723)
PORT_IO4_4	ABH_RE_M1	Monitoring relay for AI module 1 (AI_8..15) – right channel	OFF (no connection to monitor stage MAX9723)
PORT_IO4_5	ABH_LI_M1	Monitoring relay for AI module 1 (AI_8..15) – left channel	OFF (no connection to monitor stage MAX9723)
PORT_IO4_6	ABH_RE_M0	Monitoring relay for AI module 0 (AI_0..7) – right channel	OFF (no connection to monitor stage MAX9723)
PORT_IO4_7	ABH_LI_M0	Monitoring relay for AI module 0 (AI_0..7) – left channel	OFF (no connection to monitor stage MAX9723)

4.3.2 AI section (AI_16..31) AC/DC coupling, attenuation, headphone output

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	29h	52h	Control of port 0..5 with positive logic (via TBD62083A), outputs to be configured as source drivers; => Register 28h = 11h (Default)

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	REL_CH7_ACDC_M2	AC/DC coupling AI_23+	Coupling: AC
PORT_IO0_1	REL_CH6_ACDC_M2	AC/DC coupling AI_22+	Coupling: AC
PORT_IO0_2	REL_CH5_ACDC_M2	AC/DC coupling AI_21+	Coupling: AC
PORT_IO0_3	REL_CH4_ACDC_M2	AC/DC coupling AI_20+	Coupling: AC
PORT_IO0_4	REL_CH3_ACDC_M2	AC/DC coupling AI_19+	Coupling: AC
PORT_IO0_5	REL_CH2_ACDC_M2	AC/DC coupling AI_18+	Coupling: AC
PORT_IO0_6	REL_CH1_ACDC_M2	AC/DC coupling AI_17+	Coupling: AC
PORT_IO0_7	REL_CH0_ACDC_M2	AC/DC coupling AI_16+	Coupling: AC
PORT_IO1_0	REL_7_M2	Attenuation AI_23+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_1	REL_6_M2	Attenuation AI_22+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_2	REL_5_M2	Attenuation AI_21+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_3	REL_4_M2	Attenuation AI_20+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_4	REL_3_M2	Attenuation AI_19+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_5	REL_2_M2	Attenuation AI_18+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_6	REL_1_M2	Attenuation AI_17+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO1_7	REL_0_M2	Attenuation AI_16+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO2_0	REL_CH0_ACDC_M3	AC/DC coupling AI_24+	Coupling: AC
PORT_IO2_1	REL_CH1_ACDC_M3	AC/DC coupling AI_25+	Coupling: AC
PORT_IO2_2	REL_CH2_ACDC_M3	AC/DC coupling AI_26+	Coupling: AC
PORT_IO2_3	REL_CH3_ACDC_M3	AC/DC coupling AI_27+	Coupling: AC
PORT_IO2_4	REL_CH4_ACDC_M3	AC/DC coupling AI_28+	Coupling: AC
PORT_IO2_5	REL_CH5_ACDC_M3	AC/DC coupling AI_29+	Coupling: AC
PORT_IO2_6	REL_CH6_ACDC_M3	AC/DC coupling AI_30+	Coupling: AC
PORT_IO2_7	REL_CH7_ACDC_M3	AC/DC coupling AI_31+	Coupling: AC

Port PCA9698	Signal in schematic	Description	Default
PORT_IO3_0	REL_0_M3	Attenuation AI_24+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_1	REL_1_M3	Attenuation AI_25+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_2	REL_2_M3	Attenuation AI_26+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_3	REL_3_M3	Attenuation AI_27+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_4	REL_4_M3	Attenuation AI_28+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_5	REL_5_M3	Attenuation AI_29+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_6	REL_6_M3	Attenuation AI_30+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO3_7	REL_7_M3	Attenuation AI_31+ (0dB/-36dB)	Attenuation: -36dB
PORT_IO4_0	ABH_LI_KOPFH	Monitoring signal at the output of MAX9723 to the headphone – left channel	OFF (connection between monitor stage and STB19 open)
PORT_IO4_1	ABH_RE_KOPFH	Monitoring signal at the output of MAX9723 to the headphone – right channel	OFF (connection between monitor stage and STB19 open)
PORT_IO4_2	reserved		
PORT_IO4_3	reserved		
PORT_IO4_4	reserved		
PORT_IO4_5	reserved		
PORT_IO4_6	reserved		
PORT_IO4_7	reserved		

4.3.3 AO section s.e./diff switchover, mute function, switchable power lines

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	13h	26h	Control of port 0..2 with positive logic (via TBD62083A), outputs to be configured as source drivers; => Register 28h = 11h (Default)

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	AO_REL_7_SEDIFF	Output AO_H± single ended/differential	single ended (AO_H- = GND_AO)
PORT_IO0_1	AO_REL_6_SEDIFF	Output AO_G± single ended/differential	single ended (AO_G- = GND_AO)
PORT_IO0_2	AO_REL_5_SEDIFF	Output AO_F± single ended/differential	single ended (AO_F- = GND_AO)
PORT_IO0_3	AO_REL_4_SEDIFF	Output AO_E± single ended/differential	single ended (AO_E- = GND_AO)
PORT_IO0_4	AO_REL_3_SEDIFF	Output AO_D± single ended/differential	single ended (AO_D- = GND_AO)
PORT_IO0_5	AO_REL_2_SEDIFF	Output AO_C± single ended/differential	single ended (AO_C- = GND_AO)
PORT_IO0_6	AO_REL_1_SEDIFF	Output AO_B± single ended/differential	single ended (AO_B- = GND_AO)
PORT_IO0_7	AO_REL_0_SEDIFF	Output AO_A± single ended/differential	single ended (AO_A- = GND_AO)
PORT_IO1_0	AO_REL_7_MUTE	Mute function AO_H±	Mute = OFF
PORT_IO1_1	AO_REL_6_MUTE	Mute function AO_G±	Mute = OFF
PORT_IO1_2	AO_REL_5_MUTE	Mute function AO_F±	Mute = OFF
PORT_IO1_3	AO_REL_4_MUTE	Mute function AO_E±	Mute = OFF
PORT_IO1_4	AO_REL_3_MUTE	Mute function AO_D±	Mute = OFF
PORT_IO1_5	AO_REL_2_MUTE	Mute function AO_C±	Mute = OFF
PORT_IO1_6	AO_REL_1_MUTE	Mute function AO_B±	Mute = OFF
PORT_IO1_7	AO_REL_0_MUTE	Mute function AO_A±	Mute = OFF
PORT_IO2_0	REL_12V_1_INT	Switchable 12 V power line from PC (Switch 1)	OFF
PORT_IO2_1	REL_VCC_1_INT	Switchable 5 V power line from PC (Switch 1)	OFF
PORT_IO2_2	REL_12V_2_INT	Switchable 12 V power line from PC (Switch 2)	OFF
PORT_IO2_3	REL_VCC_2_INT	Switchable 5 V power line from PC (Switch 2)	OFF

Port PCA9698	Signal in schematic	Description	Default
PORT_IO2_4	REL_12V_4_INT	Switchable 12 V power line from PC (Switch 4)	OFF
PORT_IO2_5	REL_VCC_4_INT	Switchable 5 V power line from PC (Switch 4)	OFF
PORT_IO2_6	REL_12V_3_INT	Switchable 12 V power line from PC (Switch 3)	OFF
PORT_IO2_7	REL_VCC_3_INT	Switchable 5 V power line from PC (Switch 3)	OFF
PORT_IO3_0	reserved		
PORT_IO3_1	reserved		
PORT_IO3_2	reserved		
PORT_IO3_3	reserved		
PORT_IO3_4	reserved		
PORT_IO3_5	reserved		
PORT_IO3_6	reserved		
PORT_IO3_7	reserved		
PORT_IO4_0	reserved		
PORT_IO4_1	reserved		
PORT_IO4_2	reserved		
PORT_IO4_3	reserved		
PORT_IO4_4	reserved		
PORT_IO4_5	reserved		
PORT_IO4_6	reserved		
PORT_IO4_7	reserved		

4.3.4 AO section disabling analog output at LTC6090-5

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	12h	24h	Control of port 0 with negative logic, outputs to be configured as sink drivers; => Register 28h = 11h (Default)

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	AO_OUT3_B_EN	Analog output AO_H± ON/OFF (LTC6090-5)	Output disabled
PORT_IO0_1	AO_OUT3_A_EN	Analog output AO_G± ON/OFF (LTC6090-5)	Output disabled
PORT_IO0_2	AO_OUT2_B_EN	Analog output AO_F± ON/OFF (LTC6090-5)	Output disabled
PORT_IO0_3	AO_OUT2_A_EN	Analog output AO_E± ON/OFF (LTC6090-5)	Output disabled
PORT_IO0_4	AO_OUT1_B_EN	Analog output AO_D± ON/OFF (LTC6090-5)	Output disabled
PORT_IO0_5	AO_OUT1_A_EN	Analog output AO_C± ON/OFF (LTC6090-5)	Output disabled
PORT_IO0_6	AO_OUT0_B_EN	Analog output AO_B± ON/OFF (LTC6090-5)	Output disabled
PORT_IO0_7	AO_OUT0_A_EN	Analog output AO_A± ON/OFF (LTC6090-5)	Output disabled
PORT_IO1_0	reserved		
PORT_IO1_1	reserved		
PORT_IO1_2	reserved		
PORT_IO1_3	reserved		
PORT_IO1_4	reserved		
PORT_IO1_5	reserved		
PORT_IO1_6	reserved		
PORT_IO1_7	reserved		
PORT_IO2_0	reserved		
PORT_IO2_1	reserved		
PORT_IO2_2	reserved		
PORT_IO2_3	reserved		
PORT_IO2_4	reserved		
PORT_IO2_5	reserved		
PORT_IO2_6	reserved		
PORT_IO2_7	reserved		

Port PCA9698	Signal in schematic	Description	Default
PORT_IO3_0	reserved		
PORT_IO3_1	reserved		
PORT_IO3_2	reserved		
PORT_IO3_3	reserved		
PORT_IO3_4	reserved		
PORT_IO3_5	reserved		
PORT_IO3_6	reserved		
PORT_IO3_7	reserved		
PORT_IO4_0	reserved		
PORT_IO4_1	reserved		
PORT_IO4_2	reserved		
PORT_IO4_3	reserved		
PORT_IO4_4	reserved		
PORT_IO4_5	reserved		
PORT_IO4_6	reserved		
PORT_IO4_7	reserved		

4.3.5 Monitoring stage with headphone amplifier

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
MAX9723	4Ch	98h	

Each AI channel can be switched to the stereo headphone amplifier of type MAX9723. You are free to select which channel should be switched to the left resp. right channel of the MAX9723. At the output of the MAX9723 the headphone can be connected directly.

See also datasheets under:

https://www.maximintegrated.com/en/products/analog/audio/MAX9723.html

4.3.6 AI module 0, 8 channel multiplexer

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCF8574	20h	40h	Control of the 8-channel multiplexer with positive logic (A2..0)

Port PCF8574	Signal in schematic	Description	Default
PORT_P0	ABH_R_A0_M0	8 channel multiplexer AI module 0 right (DG408), bit A0	Channel 1 of AI module 0 to relay stage (Li_INT_M0)
PORT_P1	ABH_R_A1_M0	8 channel multiplexer AI module 0 right (DG408), bit A1	
PORT_P2	ABH_R_A2_M0	8 channel multiplexer AI module 0 right (DG408), bit A2	
PORT_P3	ABH_L_A0_M0	8 channel multiplexer AI module 0 left (DG408), bit A0	Channel 1 of AI module 0 to relay stage (Re_INT_M0)
PORT_P4	ABH_L_A1_M0	8 channel multiplexer AI module 0 left (DG408), bit A1	
PORT_P5	ABH_L_A2_M0	8 channel multiplexer AI module 0 left (DG408), bit A2	
PORT_P6	reserved		
PORT_P7	reserved		

4.3.7 AI module 0 (AI_0..4), digital filter stage

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	22h	44h	Control of port 0..5 with negative logic, outputs to be configured as sink drivers; => Register 28h = 00h

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	CH_4_F0_M0	Digital filter stage AI_4 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO0_1	CH_4_F1_M0	Digital filter stage AI_4 (LTC1564a), bit F1	
PORT_IO0_2	CH_4_F2_M0	Digital filter stage AI_4 (LTC1564a), bit F2	
PORT_IO0_3	CH_4_F3_M0	Digital filter stage AI_4 (LTC1564a), bit F3	
PORT_IO0_4	CH_4_G0_M0	Digital filter stage AI_4 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO0_5	CH_4_G1_M0	Digital filter stage AI_4 (LTC1564a), bit G1	
PORT_IO0_6	CH_4_G2_M0	Digital filter stage AI_4 (LTC1564a), bit G2	
PORT_IO0_7	CH_4_G3_M0	Digital filter stage AI_4 (LTC1564a), bit G3	
PORT_IO1_0	CH_3_F0_M0	Digital filter stage AI_3 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO1_1	CH_3_F1_M0	Digital filter stage AI_3 (LTC1564a), bit F1	
PORT_IO1_2	CH_3_F2_M0	Digital filter stage AI_3 (LTC1564a), bit F2	
PORT_IO1_3	CH_3_F3_M0	Digital filter stage AI_3 (LTC1564a), bit F3	
PORT_IO1_4	CH_3_G0_M0	Digital filter stage AI_3 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO1_5	CH_3_G1_M0	Digital filter stage AI_3 (LTC1564a), bit G1	
PORT_IO1_6	CH_3_G2_M0	Digital filter stage AI_3 (LTC1564a), bit G2	
PORT_IO1_7	CH_3_G3_M0	Digital filter stage AI_3 (LTC1564a), bit G3	
PORT_IO2_0	CH_0_F0_M0	Digital filter stage AI_0 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO2_1	CH_0_F1_M0	Digital filter stage AI_0 (LTC1564a), bit F1	
PORT_IO2_2	CH_0_F2_M0	Digital filter stage AI_0 (LTC1564a), bit F2	
PORT_IO2_3	CH_0_F3_M0	Digital filter stage AI_0 (LTC1564a), bit F3	

Port PCA9698	Signal in schematic	Description	Default
PORT_IO2_4	CH_0_G3_M0	Digital filter stage AI_0 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO2_5	CH_0_G2_M0	Digital filter stage AI_0 (LTC1564a), bit G2	
PORT_IO2_6	CH_0_G1_M0	Digital filter stage AI_0 (LTC1564a), bit G1	
PORT_IO2_7	CH_0_G0_M0	Digital filter stage AI_0 (LTC1564a), bit G0	
PORT_IO3_0	CH_1_F3_M0	Digital filter stage AI_1 (LTC1564a), bit F3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO3_1	CH_1_F2_M0	Digital filter stage AI_1 (LTC1564a), bit F2	
PORT_IO3_2	CH_1_F1_M0	Digital filter stage AI_1 (LTC1564a), bit F1	
PORT_IO3_3	CH_1_F0_M0	Digital filter stage AI_1 (LTC1564a), bit F0	
PORT_IO3_4	CH_1_G3_M0	Digital filter stage AI_1 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO3_5	CH_1_G2_M0	Digital filter stage AI_1 (LTC1564a), bit G2	
PORT_IO3_6	CH_1_G1_M0	Digital filter stage AI_1 (LTC1564a), bit G1	
PORT_IO3_7	CH_1_G0_M0	Digital filter stage AI_1 (LTC1564a), bit G0	
PORT_IO4_0	CH_2_F3_M0	Digital filter stage AI_2 (LTC1564a), bit F3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO4_1	CH_2_F2_M0	Digital filter stage AI_2 (LTC1564a), bit F2	
PORT_IO4_2	CH_2_F1_M0	Digital filter stage AI_2 (LTC1564a), bit F1	
PORT_IO4_3	CH_2_F0_M0	Digital filter stage AI_2 (LTC1564a), bit F0	
PORT_IO4_4	CH_2_G3_M0	Digital filter stage AI_2 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO4_5	CH_2_G2_M0	Digital filter stage AI_2 (LTC1564a), bit G2	
PORT_IO4_6	CH_2_G1_M0	Digital filter stage AI_2 (LTC1564a), bit G1	
PORT_IO4_7	CH_2_G0_M0	Digital filter stage AI_2 (LTC1564a), bit G0	

4.3.8 AI module 0 (AI_5..7), digital filter stage, monitoring stage filter

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	23h	46h	Control of port 0..2 with negative logic, outputs to be configured as sink drivers; Control of port 3..4 with positive logic, outputs to be configured as source drivers => Register 28h = C0h

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	CH_7_F0_M0	Digital filter stage AI_7 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO0_1	CH_7_F1_M0	Digital filter stage AI_7 (LTC1564a), bit F1	
PORT_IO0_2	CH_7_F2_M0	Digital filter stage AI_7 (LTC1564a), bit F2	
PORT_IO0_3	CH_7_F3_M0	Digital filter stage AI_7 (LTC1564a), bit F3	
PORT_IO0_4	CH_7_G0_M0	Digital filter stage AI_7 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO0_5	CH_7_G1_M0	Digital filter stage AI_7 (LTC1564a), bit G1	
PORT_IO0_6	CH_7_G2_M0	Digital filter stage AI_7 (LTC1564a), bit G2	
PORT_IO0_7	CH_7_G3_M0	Digital filter stage AI_7 (LTC1564a), bit G3	
PORT_IO1_0	CH_6_F0_M0	Digital filter stage AI_6 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO1_1	CH_6_F1_M0	Digital filter stage AI_6 (LTC1564a), bit F1	
PORT_IO1_2	CH_6_F2_M0	Digital filter stage AI_6 (LTC1564a), bit F2	
PORT_IO1_3	CH_6_F3_M0	Digital filter stage AI_6 (LTC1564a), bit F3	
PORT_IO1_4	CH_6_G0_M0	Digital filter stage AI_6 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO1_5	CH_6_G1_M0	Digital filter stage AI_6 (LTC1564a), bit G1	
PORT_IO1_6	CH_6_G2_M0	Digital filter stage AI_6 (LTC1564a), bit G2	
PORT_IO1_7	CH_6_G3_M0	Digital filter stage AI_6 (LTC1564a), bit G3	
PORT_IO2_0	CH_5_F0_M0	Digital filter stage AI_5 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO2_1	CH_5_F1_M0	Digital filter stage AI_5 (LTC1564a), bit F1	
PORT_IO2_2	CH_5_F2_M0	Digital filter stage AI_5 (LTC1564a), bit F2	
PORT_IO2_3	CH_5_F3_M0	Digital filter stage AI_5 (LTC1564a), bit F3	

Port PCA9698	Signal in schematic	Description	Default
PORT_IO2_4	CH_5_G3_M0	Digital filter stage AI_5 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO2_5	CH_5_G2_M0	Digital filter stage AI_5 (LTC1564a), bit G2	
PORT_IO2_6	CH_5_G1_M0	Digital filter stage AI_5 (LTC1564a), bit G1	
PORT_IO2_7	CH_5_G0_M0	Digital filter stage AI_5 (LTC1564a), bit G0	
PORT_IO3_0	ABH_Re_G3	Monitoring stage M0 filter right (LTC1564a), bit G3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO3_1	ABH_Re_G2	Monitoring stage M0 filter right (LTC1564a), bit G2	
PORT_IO3_2	ABH_Re_G1	Monitoring stage M0 filter right (LTC1564a), bit G1	
PORT_IO3_3	ABH_Re_G0	Monitoring stage M0 filter right (LTC1564a), bit G0	
PORT_IO3_4	ABH_Re_F3	Monitoring stage M0 filter right (LTC1564a), bit F3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO3_5	ABH_Re_F2	Monitoring stage M0 filter right (LTC1564a), bit F2	
PORT_IO3_6	ABH_Re_F1	Monitoring stage M0 filter right (LTC1564a), bit F1	
PORT_IO3_7	ABH_Re_F0	Monitoring stage M0 filter right (LTC1564a), bit F0	
PORT_IO4_0	ABH_Li_G3	Monitoring stage M0 filter left (LTC1564a), bit G3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO4_1	ABH_Li_G2	Monitoring stage M0 filter left (LTC1564a), bit G2	
PORT_IO4_2	ABH_Li_G1	Monitoring stage M0 filter left (LTC1564a), bit G1	
PORT_IO4_3	ABH_Li_G0	Monitoring stage M0 filter left (LTC1564a), bit G0	
PORT_IO4_4	ABH_Li_F3	Monitoring stage M0 filter left (LTC1564a), bit F3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO4_5	ABH_Li_F2	Monitoring stage M0 filter left (LTC1564a), bit F2	
PORT_IO4_6	ABH_Li_F1	Monitoring stage M0 filter left (LTC1564a), bit F1	
PORT_IO4_7	ABH_Li_F0	Monitoring stage M0 filter left (LTC1564a), bit F0	

4.3.9 AI module 1 (AI_8..12), digital filter stage

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	24h	48h	Control of port 0..5 with negative logic, outputs to be configured as sink drivers; => Register 28h = C0h

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	CH_4_F0_M1	Digital filter stage AI_12 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO0_1	CH_4_F1_M1	Digital filter stage AI_12 (LTC1564a), bit F1	
PORT_IO0_2	CH_4_F2_M1	Digital filter stage AI_12 (LTC1564a), bit F2	
PORT_IO0_3	CH_4_F3_M1	Digital filter stage AI_12 (LTC1564a), bit F3	
PORT_IO0_4	CH_4_G0_M1	Digital filter stage AI_12 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO0_5	CH_4_G1_M1	Digital filter stage AI_12 (LTC1564a), bit G1	
PORT_IO0_6	CH_4_G2_M1	Digital filter stage AI_12 (LTC1564a), bit G2	
PORT_IO0_7	CH_4_G3_M1	Digital filter stage AI_12 (LTC1564a), bit G3	
PORT_IO1_0	CH_3_F0_M1	Digital filter stage AI_11 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO1_1	CH_3_F1_M1	Digital filter stage AI_11 (LTC1564a), bit F1	
PORT_IO1_2	CH_3_F2_M1	Digital filter stage AI_11 (LTC1564a), bit F2	
PORT_IO1_3	CH_3_F3_M1	Digital filter stage AI_11 (LTC1564a), bit F3	
PORT_IO1_4	CH_3_G0_M1	Digital filter stage AI_11 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO1_5	CH_3_G1_M1	Digital filter stage AI_11 (LTC1564a), bit G1	
PORT_IO1_6	CH_3_G2_M1	Digital filter stage AI_11 (LTC1564a), bit G2	
PORT_IO1_7	CH_3_G3_M1	Digital filter stage AI_11 (LTC1564a), bit G3	
PORT_IO2_0	CH_0_F0_M1	Digital filter stage AI_8 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO2_1	CH_0_F1_M1	Digital filter stage AI_8 (LTC1564a), bit F1	
PORT_IO2_2	CH_0_F2_M1	Digital filter stage AI_8 (LTC1564a), bit F2	
PORT_IO2_3	CH_0_F3_M1	Digital filter stage AI_8 (LTC1564a), bit F3	

Port PCA9698	Signal in schematic	Description	Default
PORT_IO2_4	CH_0_G3_M1	Digital filter stage AI_8 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO2_5	CH_0_G2_M1	Digital filter stage AI_8 (LTC1564a), bit G2	
PORT_IO2_6	CH_0_G1_M1	Digital filter stage AI_8 (LTC1564a), bit G1	
PORT_IO2_7	CH_0_G0_M1	Digital filter stage AI_8 (LTC1564a), bit G0	
PORT_IO3_0	CH_1_F3_M1	Digital filter stage AI_9 (LTC1564a), bit F3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO3_1	CH_1_F2_M1	Digital filter stage AI_9 (LTC1564a), bit F2	
PORT_IO3_2	CH_1_F1_M1	Digital filter stage AI_9 (LTC1564a), bit F1	
PORT_IO3_3	CH_1_F0_M1	Digital filter stage AI_9 (LTC1564a), bit F0	
PORT_IO3_4	CH_1_G3_M1	Digital filter stage AI_9 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO3_5	CH_1_G2_M1	Digital filter stage AI_9 (LTC1564a), bit G2	
PORT_IO3_6	CH_1_G1_M1	Digital filter stage AI_9 (LTC1564a), bit G1	
PORT_IO3_7	CH_1_G0_M1	Digital filter stage AI_9 (LTC1564a), bit G0	
PORT_IO4_0	CH_2_F3_M1	Digital filter stage AI_10 (LTC1564a), bit F3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO4_1	CH_2_F2_M1	Digital filter stage AI_10 (LTC1564a), bit F2	
PORT_IO4_2	CH_2_F1_M1	Digital filter stage AI_10 (LTC1564a), bit F1	
PORT_IO4_3	CH_2_F0_M1	Digital filter stage AI_10 (LTC1564a), bit F0	
PORT_IO4_4	CH_2_G3_M1	Digital filter stage AI_10 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO4_5	CH_2_G2_M1	Digital filter stage AI_10 (LTC1564a), bit G2	
PORT_IO4_6	CH_2_G1_M1	Digital filter stage AI_10 (LTC1564a), bit G1	
PORT_IO4_7	CH_2_G0_M1	Digital filter stage AI_10 (LTC1564a), bit G0	

4.3.10 AI module 1 (AI_13..15), digital filter stage, 8 channel multiplexer

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	25h	4Ah	Control of port 0..2 with negative logic, outputs to be configured as sink drivers; Control of port 3 with positive logic, outputs to be configured as source drivers => Register 28h = C0h

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	CH_7_F0_M1	Digital filter stage AI_15 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO0_1	CH_7_F1_M1	Digital filter stage AI_15 (LTC1564a), bit F1	
PORT_IO0_2	CH_7_F2_M1	Digital filter stage AI_15 (LTC1564a), bit F2	
PORT_IO0_3	CH_7_F3_M1	Digital filter stage AI_15 (LTC1564a), bit F3	
PORT_IO0_4	CH_7_G0_M1	Digital filter stage AI_15 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO0_5	CH_7_G1_M1	Digital filter stage AI_15 (LTC1564a), bit G1	
PORT_IO0_6	CH_7_G2_M1	Digital filter stage AI_15 (LTC1564a), bit G2	
PORT_IO0_7	CH_7_G3_M1	Digital filter stage AI_15 (LTC1564a), bit G3	
PORT_IO1_0	CH_6_F0_M1	Digital filter stage AI_14 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO1_1	CH_6_F1_M1	Digital filter stage AI_14 (LTC1564a), bit F1	
PORT_IO1_2	CH_6_F2_M1	Digital filter stage AI_14 (LTC1564a), bit F2	
PORT_IO1_3	CH_6_F3_M1	Digital filter stage AI_14 (LTC1564a), bit F3	
PORT_IO1_4	CH_6_G0_M1	Digital filter stage AI_14 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO1_5	CH_6_G1_M1	Digital filter stage AI_14 (LTC1564a), bit G1	
PORT_IO1_6	CH_6_G2_M1	Digital filter stage AI_14 (LTC1564a), bit G2	
PORT_IO1_7	CH_6_G3_M1	Digital filter stage AI_14 (LTC1564a), bit G3	
PORT_IO2_0	CH_5_F0_M1	Digital filter stage AI_13 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO2_1	CH_5_F1_M1	Digital filter stage AI_13 (LTC1564a), bit F1	
PORT_IO2_2	CH_5_F2_M1	Digital filter stage AI_13 (LTC1564a), bit F2	
PORT_IO2_3	CH_5_F3_M1	Digital filter stage AI_13 (LTC1564a), bit F3	

Port PCA9698	Signal in schematic	Description	Default
PORT_IO2_4	CH_5_G3_M1	Digital filter stage AI_13 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO2_5	CH_5_G2_M1	Digital filter stage AI_13 (LTC1564a), bit G2	
PORT_IO2_6	CH_5_G1_M1	Digital filter stage AI_13 (LTC1564a), bit G1	
PORT_IO2_7	CH_5_G0_M1	Digital filter stage AI_13 (LTC1564a), bit G0	
PORT_IO3_0	ABH_R_A0_M1	8 channel multiplexer AI module 1 right (DG408), bit A0	Channel 1 of AI module 1 to relay stage (Li_INT_M1)
PORT_IO3_1	ABH_R_A1_M1	8 channel multiplexer AI module 1 right (DG408), bit A1	
PORT_IO3_2	ABH_R_A2_M1	8 channel multiplexer AI module 1 right (DG408), bit A2	
PORT_IO3_3	ABH_L_A0_M1	8 channel multiplexer AI module 1 left (DG408), bit A0	Channel 1 of AI module 1 to relay stage (Re_INT_M1)
PORT_IO3_4	ABH_L_A1_M1	8 channel multiplexer AI module 1 left (DG408), bit A1	
PORT_IO3_5	ABH_L_A2_M1	8 channel multiplexer AI module 1 left (DG408), bit A2	
PORT_IO3_6	reserved		
PORT_IO3_7	reserved		
PORT_IO4_0	reserved		
PORT_IO4_1	reserved		
PORT_IO4_2	reserved		
PORT_IO4_3	reserved		
PORT_IO4_4	reserved		
PORT_IO4_5	reserved		
PORT_IO4_6	reserved		
PORT_IO4_7	reserved		

4.3.11 AI module 2 (AI_16..20), digital filter stage

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	26h	4Ch	Control of port 0..5 with negative logic, outputs to be configured as sink drivers; => Register 28h = 00h

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	CH_4_F0_M2	Digital filter stage AI_20 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO0_1	CH_4_F1_M2	Digital filter stage AI_20 (LTC1564a), bit F1	
PORT_IO0_2	CH_4_F2_M2	Digital filter stage AI_20 (LTC1564a), bit F2	
PORT_IO0_3	CH_4_F3_M2	Digital filter stage AI_20 (LTC1564a), bit F3	
PORT_IO0_4	CH_4_G0_M2	Digital filter stage AI_20 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO0_5	CH_4_G1_M2	Digital filter stage AI_20 (LTC1564a), bit G1	
PORT_IO0_6	CH_4_G2_M2	Digital filter stage AI_20 (LTC1564a), bit G2	
PORT_IO0_7	CH_4_G3_M2	Digital filter stage AI_20 (LTC1564a), bit G3	
PORT_IO1_0	CH_3_F0_M2	Digital filter stage AI_19 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO1_1	CH_3_F1_M2	Digital filter stage AI_19 (LTC1564a), bit F1	
PORT_IO1_2	CH_3_F2_M2	Digital filter stage AI_19 (LTC1564a), bit F2	
PORT_IO1_3	CH_3_F3_M2	Digital filter stage AI_19 (LTC1564a), bit F3	
PORT_IO1_4	CH_3_G0_M2	Digital filter stage AI_19 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO1_5	CH_3_G1_M2	Digital filter stage AI_19 (LTC1564a), bit G1	
PORT_IO1_6	CH_3_G2_M2	Digital filter stage AI_19 (LTC1564a), bit G2	
PORT_IO1_7	CH_3_G3_M2	Digital filter stage AI_19 (LTC1564a), bit G3	
PORT_IO2_0	CH_0_F0_M2	Digital filter stage AI_16 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO2_1	CH_0_F1_M2	Digital filter stage AI_16 (LTC1564a), bit F1	
PORT_IO2_2	CH_0_F2_M2	Digital filter stage AI_16 (LTC1564a), bit F2	
PORT_IO2_3	CH_0_F3_M2	Digital filter stage AI_16 (LTC1564a), bit F3	

Port PCA9698	Signal in schematic	Description	Default
PORT_IO2_4	CH_0_G3_M2	Digital filter stage AI_16 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO2_5	CH_0_G2_M2	Digital filter stage AI_16 (LTC1564a), bit G2	
PORT_IO2_6	CH_0_G1_M2	Digital filter stage AI_16 (LTC1564a), bit G1	
PORT_IO2_7	CH_0_G0_M2	Digital filter stage AI_16 (LTC1564a), bit G0	
PORT_IO3_0	CH_1_F3_M2	Digital filter stage AI_17 (LTC1564a), bit F3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO3_1	CH_1_F2_M2	Digital filter stage AI_17 (LTC1564a), bit F2	
PORT_IO3_2	CH_1_F1_M2	Digital filter stage AI_17 (LTC1564a), bit F1	
PORT_IO3_3	CH_1_F0_M2	Digital filter stage AI_17 (LTC1564a), bit F0	
PORT_IO3_4	CH_1_G3_M2	Digital filter stage AI_17 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO3_5	CH_1_G2_M2	Digital filter stage AI_17 (LTC1564a), bit G2	
PORT_IO3_6	CH_1_G1_M2	Digital filter stage AI_17 (LTC1564a), bit G1	
PORT_IO3_7	CH_1_G0_M2	Digital filter stage AI_17 (LTC1564a), bit G0	
PORT_IO4_0	CH_2_F3_M2	Digital filter stage AI_18 (LTC1564a), bit F3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO4_1	CH_2_F2_M2	Digital filter stage AI_18 (LTC1564a), bit F2	
PORT_IO4_2	CH_2_F1_M2	Digital filter stage AI_18 (LTC1564a), bit F1	
PORT_IO4_3	CH_2_F0_M2	Digital filter stage AI_18 (LTC1564a), bit F0	
PORT_IO4_4	CH_2_G3_M2	Digital filter stage AI_18 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO4_5	CH_2_G2_M2	Digital filter stage AI_18 (LTC1564a), bit G2	
PORT_IO4_6	CH_2_G1_M2	Digital filter stage AI_18 (LTC1564a), bit G1	
PORT_IO4_7	CH_2_G0_M2	Digital filter stage AI_18 (LTC1564a), bit G0	

4.3.12 AI module 2 (AI_21..23), digital filter stage, 8 channel multiplexer

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	27h	4Eh	Control of port 0..2 with negative logic, outputs to be configured as sink drivers; Control of port 3 with positive logic, outputs to be configured as source drivers => Register 28h = C0h

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	CH_7_F0_M2	Digital filter stage AI_23 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO0_1	CH_7_F1_M2	Digital filter stage AI_23 (LTC1564a), bit F1	
PORT_IO0_2	CH_7_F2_M2	Digital filter stage AI_23 (LTC1564a), bit F2	
PORT_IO0_3	CH_7_F3_M2	Digital filter stage AI_23 (LTC1564a), bit F3	
PORT_IO0_4	CH_7_G0_M2	Digital filter stage AI_23 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO0_5	CH_7_G1_M2	Digital filter stage AI_23 (LTC1564a), bit G1	
PORT_IO0_6	CH_7_G2_M2	Digital filter stage AI_23 (LTC1564a), bit G2	
PORT_IO0_7	CH_7_G3_M2	Digital filter stage AI_23 (LTC1564a), bit G3	
PORT_IO1_0	CH_6_F0_M2	Digital filter stage AI_22 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO1_1	CH_6_F1_M2	Digital filter stage AI_22 (LTC1564a), bit F1	
PORT_IO1_2	CH_6_F2_M2	Digital filter stage AI_22 (LTC1564a), bit F2	
PORT_IO1_3	CH_6_F3_M2	Digital filter stage AI_22 (LTC1564a), bit F3	
PORT_IO1_4	CH_6_G0_M2	Digital filter stage AI_22 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO1_5	CH_6_G1_M2	Digital filter stage AI_22 (LTC1564a), bit G1	
PORT_IO1_6	CH_6_G2_M2	Digital filter stage AI_22 (LTC1564a), bit G2	
PORT_IO1_7	CH_6_G3_M2	Digital filter stage AI_22 (LTC1564a), bit G3	

Port PCA9698	Signal in schematic	Description	Default
	CH_5_F0_M2	Digital filter stage AI_21 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO2_1	CH_5_F1_M2	Digital filter stage AI_21 (LTC1564a), bit F1	
PORT_IO2_0 PORT_IO2_2	CH_5_F2_M2	Digital filter stage AI_21 (LTC1564a), bit F2	
PORT_IO2_3	CH_5_F3_M2	Digital filter stage AI_21 (LTC1564a), bit F3	
PORT_IO2_4	CH_5_G3_M2	Digital filter stage AI_21 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO2_5	CH_5_G2_M2	Digital filter stage AI_21 (LTC1564a), bit G2	
PORT_IO2_6	CH_5_G1_M2	Digital filter stage AI_21 (LTC1564a), bit G1	
PORT_IO2_7	CH_5_G0_M2	Digital filter stage AI_21 (LTC1564a), bit G0	
PORT_IO3_0	ABH_R_A0_M2	8 channel multiplexer AI module 2 right (DG408), bit A0	Channel 1 of AI module 2 to relay stage (Li_INT_M2)
PORT_IO3_1	ABH_R_A1_M2	8 channel multiplexer AI module 2 right (DG408), bit A1	
PORT_IO3_2	ABH_R_A2_M2	8 channel multiplexer AI module 2 right (DG408), bit A2	
PORT_IO3_3	ABH_L_A0_M2	8 channel multiplexer AI module 2 left (DG408), bit A0	Channel 1 of AI module 2 to relay stage (Re_INT_M2)
PORT_IO3_4	ABH_L_A1_M2	8 channel multiplexer AI module 2 left (DG408), bit A1	
PORT_IO3_5	ABH_L_A2_M2	8 channel multiplexer AI module 2 left (DG408), bit A2	
PORT_IO3_6	reserved		
PORT_IO3_7	reserved		
PORT_IO4_0	reserved		
PORT_IO4_1	reserved		
PORT_IO4_2	reserved		
PORT_IO4_3	reserved		
PORT_IO4_4	reserved		
PORT_IO4_5	reserved		
PORT_IO4_6	reserved		
PORT_IO4_7	reserved		

4.3.13 AI module 3 (AI_24..28), digital filter stage

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	10h	20h	Control of port 0..5 with negative logic, outputs to be configured as sink drivers; => Register 28h = 00h

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	CH_4_F0_M3	Digital filter stage AI_28 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO0_1	CH_4_F1_M3	Digital filter stage AI_28 (LTC1564a), bit F1	
PORT_IO0_2	CH_4_F2_M3	Digital filter stage AI_28 (LTC1564a), bit F2	
PORT_IO0_3	CH_4_F3_M3	Digital filter stage AI_28 (LTC1564a), bit F3	
PORT_IO0_4	CH_4_G0_M3	Digital filter stage AI_28 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO0_5	CH_4_G1_M3	Digital filter stage AI_28 (LTC1564a), bit G1	
PORT_IO0_6	CH_4_G2_M3	Digital filter stage AI_28 (LTC1564a), bit G2	
PORT_IO0_7	CH_4_G3_M3	Digital filter stage AI_28 (LTC1564a), bit G3	
PORT_IO1_0	CH_3_F0_M3	Digital filter stage AI_27 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO1_1	CH_3_F1_M3	Digital filter stage AI_27 (LTC1564a), bit F1	
PORT_IO1_2	CH_3_F2_M3	Digital filter stage AI_27 (LTC1564a), bit F2	
PORT_IO1_3	CH_3_F3_M3	Digital filter stage AI_27 (LTC1564a), bit F3	
PORT_IO1_4	CH_3_G0_M3	Digital filter stage AI_27 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO1_5	CH_3_G1_M3	Digital filter stage AI_27 (LTC1564a), bit G1	
PORT_IO1_6	CH_3_G2_M3	Digital filter stage AI_27 (LTC1564a), bit G2	
PORT_IO1_7	CH_3_G3_M3	Digital filter stage AI_27 (LTC1564a), bit G3	
PORT_IO2_0	CH_0_F0_M3	Digital filter stage AI_24 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO2_1	CH_0_F1_M3	Digital filter stage AI_24 (LTC1564a), bit F1	
PORT_IO2_2	CH_0_F2_M3	Digital filter stage AI_24 (LTC1564a), bit F2	
PORT_IO2_3	CH_0_F3_M3	Digital filter stage AI_24 (LTC1564a), bit F3	

Port PCA9698	Signal in schematic	Description	Default
PORT_IO2_4	CH_0_G3_M3	Digital filter stage AI_24 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO2_5	CH_0_G2_M3	Digital filter stage AI_24 (LTC1564a), bit G2	
PORT_IO2_6	CH_0_G1_M3	Digital filter stage AI_24 (LTC1564a), bit G1	
PORT_IO2_7	CH_0_G0_M3	Digital filter stage AI_24 (LTC1564a), bit G0	
PORT_IO3_0	CH_1_F3_M3	Digital filter stage AI_25 (LTC1564a), bit F3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO3_1	CH_1_F2_M3	Digital filter stage AI_25 (LTC1564a), bit F2	
PORT_IO3_2	CH_1_F1_M3	Digital filter stage AI_25 (LTC1564a), bit F1	
PORT_IO3_3	CH_1_F0_M3	Digital filter stage AI_25 (LTC1564a), bit F0	
PORT_IO3_4	CH_1_G3_M3	Digital filter stage AI_25 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO3_5	CH_1_G2_M3	Digital filter stage AI_25 (LTC1564a), bit G2	
PORT_IO3_6	CH_1_G1_M3	Digital filter stage AI_25 (LTC1564a), bit G1	
PORT_IO3_7	CH_1_G0_M3	Digital filter stage AI_25 (LTC1564a), bit G0	
PORT_IO4_0	CH_2_F3_M3	Digital filter stage AI_26 (LTC1564a), bit F3	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO4_1	CH_2_F2_M3	Digital filter stage AI_26 (LTC1564a), bit F2	
PORT_IO4_2	CH_2_F1_M3	Digital filter stage AI_26 (LTC1564a), bit F1	
PORT_IO4_3	CH_2_F0_M3	Digital filter stage AI_26 (LTC1564a), bit F0	
PORT_IO4_4	CH_2_G3_M3	Digital filter stage AI_26 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO4_5	CH_2_G2_M3	Digital filter stage AI_26 (LTC1564a), bit G2	
PORT_IO4_6	CH_2_G1_M3	Digital filter stage AI_26 (LTC1564a), bit G1	
PORT_IO4_7	CH_2_G0_M3	Digital filter stage AI_26 (LTC1564a), bit G0	

4.3.14 AI module 3 (AI_29..31), digital filter stage, 8 channel multiplexer

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	11h	22h	Control of port 0..2 with negative logic, outputs to be configured as sink drivers; Control of port 3 with positive logic, outputs to be configured as source drivers => Register 28h = C0h

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	CH_7_F0_M3	Digital filter stage AI_31 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO0_1	CH_7_F1_M3	Digital filter stage AI_31 (LTC1564a), bit F1	
PORT_IO0_2	CH_7_F2_M3	Digital filter stage AI_31 (LTC1564a), bit F2	
PORT_IO0_3	CH_7_F3_M3	Digital filter stage AI_31 (LTC1564a), bit F3	
PORT_IO0_4	CH_7_G0_M3	Digital filter stage AI_31 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO0_5	CH_7_G1_M3	Digital filter stage AI_31 (LTC1564a), bit G1	
PORT_IO0_6	CH_7_G2_M3	Digital filter stage AI_31 (LTC1564a), bit G2	
PORT_IO0_7	CH_7_G3_M3	Digital filter stage AI_31 (LTC1564a), bit G3	
PORT_IO1_0	CH_6_F0_M3	Digital filter stage AI_30 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO1_1	CH_6_F1_M3	Digital filter stage AI_30 (LTC1564a), bit F1	
PORT_IO1_2	CH_6_F2_M3	Digital filter stage AI_30 (LTC1564a), bit F2	
PORT_IO1_3	CH_6_F3_M3	Digital filter stage AI_30 (LTC1564a), bit F3	
PORT_IO1_4	CH_6_G0_M3	Digital filter stage AI_30 (LTC1564a), bit G0	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO1_5	CH_6_G1_M3	Digital filter stage AI_30 (LTC1564a), bit G1	
PORT_IO1_6	CH_6_G2_M3	Digital filter stage AI_30 (LTC1564a), bit G2	
PORT_IO1_7	CH_6_G3_M3	Digital filter stage AI_30 (LTC1564a), bit G3	

Port PCA9698	Signal in schematic	Description	Default
	CH_5_F0_M3	Digital filter stage AI_29 (LTC1564a), bit F0	Cut-off frequency: 150 kHz (Binary coded F3..0 see chap. 4.2 on page 38)
PORT_IO2_1	CH_5_F1_M3	Digital filter stage AI_29 (LTC1564a), bit F1	
PORT_IO2_0 PORT_IO2_2	CH_5_F2_M3	Digital filter stage AI_29 (LTC1564a), bit F2	
PORT_IO2_3	CH_5_F3_M3	Digital filter stage AI_29 (LTC1564a), bit F3	
PORT_IO2_4	CH_5_G3_M3	Digital filter stage AI_29 (LTC1564a), bit G3	Gain factor = 16 (Binary coded G3..0 see chap. 4.2 on page 38)
PORT_IO2_5	CH_5_G2_M3	Digital filter stage AI_29 (LTC1564a), bit G2	
PORT_IO2_6	CH_5_G1_M3	Digital filter stage AI_29 (LTC1564a), bit G1	
PORT_IO2_7	CH_5_G0_M3	Digital filter stage AI_29 (LTC1564a), bit G0	
PORT_IO3_0	ABH_R_A0_M3	8 channel multiplexer AI module 3 right (DG408), bit A0	Channel 1 of AI module 3 to relay stage (Li_INT_M3)
PORT_IO3_1	ABH_R_A1_M3	8 channel multiplexer AI module 3 right (DG408), bit A1	
PORT_IO3_2	ABH_R_A2_M3	8 channel multiplexer AI module 3 right (DG408), bit A2	
PORT_IO3_3	ABH_L_A0_M3	8 channel multiplexer AI module 3 left (DG408), bit A0	Channel 1 of AI module 3 to relay stage (Re_INT_M3)
PORT_IO3_4	ABH_L_A1_M3	8 channel multiplexer AI module 3 left (DG408), bit A1	
PORT_IO3_5	ABH_L_A2_M3	8 channel multiplexer AI module 3 left (DG408), bit A2	
PORT_IO3_6	reserved		
PORT_IO3_7	reserved		
PORT_IO4_0	reserved		
PORT_IO4_1	reserved		
PORT_IO4_2	reserved		
PORT_IO4_3	reserved		
PORT_IO4_4	reserved		
PORT_IO4_5	reserved		
PORT_IO4_6	reserved		
PORT_IO4_7	reserved		

4.3.15 4 channel I²C master/slave switch

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9546A	70h	E0h	

Port PCA9546A	Signal in schematic	Description	Default
SCL	SCL_MASTER	SCL to HDMI connector (STB18) incoming	–
SDA	SDA_MASTER	SDA to HDMI connector (STB18) incoming	–
SC0	SCL_BASE	SCL-Slave 0 for base board	SC0 disabled
SD0	SDA_BASE	SDA-Slave 0 for base board	SD0 disabled
SC1	SCL_ASTB3	SCL-Slave 1 for mezzanine board 3 (via JB5)	SC1 disabled
SD1	SDA_ASTB3	SDA-Slave 1 for mezzanine board 3 (via JB5)	SD1 disabled
SC2	SCL_ASTB2	SCL-Slave 2 for mezzanine board 2 (via JB4)	SC2 disabled
SD2	SDA_ASTB2	SDA-Slave 2 for mezzanine board 2 (via JB4)	SD2 disabled
SC3	SCL_ASTB1	SCL-Slave 3 for mezzanine board 1 (via JB3)	SC3 disabled
SD3	SDA_ASTB1	SDA-Slave 3 for mezzanine board 1 (via JB3)	SD3 disabled

4.3.16 I²C temperature monitoring with threshold setting and alarm output

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
LM75a	47h	9Eh	

Signal in schematic	Description	Default
SCL_BASE	SCL signal for I²C temperature sensor	–
SDA_BASE	SDA signal for I²C temperature sensor	–

4.3.17 I²C EEPROM for user-specific data

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
M24256-BR	50h	A0h	

Signal in schematic	Description	Default
SCL_BASE	SCL signal for EEPROM	–
SDA_BASE	SDA signal for EEPROM	–

4.4 Power board (ADQ-SCU-PB)

4.4.1 Relay control (U1..6): 2 high current relays, 4 standard relays

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCF8574A	39h	72h	Control of the relays with negative logic (via ULN2803)

Port PCF8574A	Signal in schematic	Description	Default
PORT_P0	Rel_U1	High current relays (12 V/100 A), channel U1	Relay open
PORT_P1	Rel_U2	High current relays (12 V/100 A), channel U2	Relay open
PORT_P2	Rel_U3	Standard relys 1 x Ein (30 V/5 A), channel U3	Relay open
PORT_P3	Rel_U4	Standard relys 1 x Ein (30 V/5 A), channel U4	Relay open
PORT_P4	Rel_U5	Standard relys 1 x Ein (30 V/5 A), channel U5	Relay open
PORT_P5	Rel_U6	Standard relys 1 x Ein (30 V/5 A), channel U6	Relay open
PORT_P6	reserved		
PORT_P7	reserved		

4.4.2 4 channel power measurement (U3..6)

Channel U3:

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
LTC2945	6Fh	DEh	Read measurement values from channel U3

Port LTC2945	Signal in schematic	Description	Default
SCL	SCL_BASE (SCL_5V)	SCL for LTC2945, channel U3	–
SDAI/SDAO	SDA_BASE (SDA_5V)	SDA for LTC2945, channel U3	–

Channel U4:

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
LTC2945	6Ch	D8h	Read measurement values from channel U4

Port LTC2945	Signal in schematic	Description	Default
SCL	SCL_BASE (SCL_5V)	SCL for LTC2945, channel U4	–
SDAI/SDAO	SDA_BASE (SDA_5V)	SDA for LTC2945, channel U4	–

Channel U5:

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
LTC2945	67h	CEh	Read measurement values from channel U5

Port LTC2945	Signal in schematic	Description	Default
SCL	SCL_BASE (SCL_5V)	SCL for LTC2945, channel U5	–
SDAI/SDAO	SDA_BASE (SDA_5V)	SDA for LTC2945, channel U5	–

Channel U6:

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
LTC2945	69h	D2h	Read measurement values from channel U6

Port LTC2945	Signal in schematic	Description	Default
SCL	SCL_BASE (SCL_5V)	SCL for LTC2945, channel U6	–
SDAI/SDAO	SDA_BASE (SDA_5V)	SDA for LTC2945, channel U6	–

4.5 Relay board (ADQ-SCU-RB)

4.5.1 Relay mezzanine board with 16 SPDT relays, 24 TTL-I/Os

I²C chip	I²C address (7 bit)	I²C address (8 bit)	Comment
PCA9698	14h	28h	Port 0..2 are input ports (positive logic) Control of port 3..4 with positive logic (via ULN2803), outputs to be configured as source drivers => Register 28h = 11h (Default)

Port PCA9698	Signal in schematic	Description	Default
PORT_IO0_0	IO0	TTL-I/Os directly connected with STR5. Each TTO-I/O can be programmed as input or output separately, outputs can be configured for sink or source operation.	Input
PORT_IO0_1	IO1		Input
PORT_IO0_2	IO2		Input
PORT_IO0_3	IO3		Input
PORT_IO0_4	IO4		Input
PORT_IO0_5	IO5		Input
PORT_IO0_6	IO6		Input
PORT_IO0_7	IO7		Input
PORT_IO1_0	IO8	TTL-I/Os directly connected with STR6. Each TTO-I/O can be programmed as input or output separately, outputs can be configured for sink or source operation.	Input
PORT_IO1_1	IO9		Input
PORT_IO1_2	IO10		Input
PORT_IO1_3	IO11		Input
PORT_IO1_4	IO12		Input
PORT_IO1_5	IO13		Input
PORT_IO1_6	IO14		Input
PORT_IO1_7	IO15		Input
PORT_IO2_0	IO16	TTL-I/Os directly connected with STR7. Each TTO-I/O can be programmed as input or output separately, outputs can be configured for sink or source operation.	Input
PORT_IO2_1	IO17		Input
PORT_IO2_2	IO18		Input
PORT_IO2_3	IO19		Input
PORT_IO2_4	IO20		Input
PORT_IO2_5	IO21		Input
PORT_IO2_6	IO22		Input
PORT_IO2_7	IO23		Input

Port PCA9698	Signal in schematic	Description	Default
PORT_IO3_0	Rel1	SPDT relays 30 V/6 A (form C), see STR1	COM connected with NC
PORT_IO3_1	Rel2	SPDT relays 30 V/6 A (form C), see STR1	COM connected with NC
PORT_IO3_2	Rel3	SPDT relays 30 V/6 A (form C), see STR1	COM connected with NC
PORT_IO3_3	Rel4	SPDT relays 30 V/6 A (form C), see STR1	COM connected with NC
PORT_IO3_4	Rel5	SPDT relays 30 V/6 A (form C), see STR2	COM connected with NC
PORT_IO3_5	Rel6	SPDT relays 30 V/6 A (form C), see STR2	COM connected with NC
PORT_IO3_6	Rel7	SPDT relays 30 V/6 A (form C), see STR2	COM connected with NC
PORT_IO3_7	Rel8	SPDT relays 30 V/6 A (form C), see STR2	COM connected with NC
PORT_IO4_0	Rel9	SPDT relays 30 V/6 A (form C), see STR3	COM connected with NC
PORT_IO4_1	Rel10	SPDT relays 30 V/6 A (form C), see STR3	COM connected with NC
PORT_IO4_2	Rel11	SPDT relays 30 V/6 A (form C), see STR3	COM connected with NC
PORT_IO4_3	Rel12	SPDT relays 30 V/6 A (form C), see STR3	COM connected with NC
PORT_IO4_4	Rel13	SPDT relays 30 V/6 A (form C), see STR4	COM connected with NC
PORT_IO4_5	Rel14	SPDT relays 30 V/6 A (form C), see STR4	COM connected with NC
PORT_IO4_6	Rel15	SPDT relays 30 V/6 A (form C), see STR4	COM connected with NC
PORT_IO4_7	Rel16	SPDT relays 30 V/6 A (form C), see STR4	COM connected with NC

5. Specifications

Conditions: T_A = 25°C if not otherwise specified; warm-up time: 30 minutes.

General

Element	Condition	Specification
Control and signal processing	recommended	ADQ-344 for analog and digital inputs/outputs, as well as control via I^2C bus
Power supply	STB16/17	+5 V / +12 V via Molex connectors from PC power supply driving ±5 V, ±15 V, ±24 V on ADQ-SCU-BB/PB/RB
Auxiliary power (switchable)	STB11..14 STB15	Power input from PC power supply via four Molex connectors. Output via relay at STB15.
Quiescent current	ADQ-SCU-BB/PB/RB relays inactive	max. +5 V: 75 mA max. +12 V: 1.2 A
Current consumption	ADQ-SCU-BB all relays active	max. +5 V: 60 mA max. +12 V: 2.6 A
	ADQ-SCU-PB all relays active	max. +5 V: 60 mA max. +12 V: 280 mA
	ADQ-SCU-RB all relays active	max. +5 V: 60 mA max. +12 V: 350 mA
Fuses for switchable auxiliary power via STB15	+5 V (F2, F4, F6, F8)	4 A (resetable, type: Polyfuse)
	+12 V (F1, F3, F5, F7)	4 A (resetable, type: Polyfuse)
Temperature range	operating	0..60 °C (standard)
Humidity	operating	20%..55% (not condensing)
Dimensions (W x D x H)	ADQ-SCU-BB	330 x 250 x 40 mm
	ADQ-SCU-PB	135 x 125 x 65 mm
	ADQ-SCU-RB	135 x 125 x 19 mm
	Total height	80 mm
Manufacturer warranty		36 months

Element	Condition	Specification
Connectors	STB1..4* STB15*	20-pin Molex Micro-Fit connector 43045-2026 Receptable housing: 43025-2010
	STB5*	16-pin Molex Micro-Fit connector 43045-1626 Receptable housing: 43025-1610
	STB6..10*	10-pin Molex Micro-Fit Stecker 43045-1026 Receptable housing: 43025-1010
	STB11..14 STB16..17	4-pin Molex power supply connectors of 8981 series (180°)
	STB18	HDMI connector, type HEC
	STB19	3-pin header, type: Phoenix Contact MCV 1,5/ 3-G-3,5 (Phoenix order no.: 1843237), Mating plug with push-in spring connection: Phoenix Contact FMC 1,5/ 3-STF-3,5 (Phoenix order no.: 1966101)
	STB20..21	BNC female connectors
	STB30..61, STB70..73	MMCX female connectors
	STB_VA, STB_VB	68-pin VHDCI female connectors
	STR1..4*	12-pin Molex Micro-Fit connector 43045-1226 Receptable housing: 43025-1210
	STR5..7*	10-pin Molex Micro-Fit connector 43045-1026 Receptable housing: 43025-1010
	ST1..8	Single-pole high current connector of type: Würth Electronic REDCUBE Direct Plug Terminal WP-PLUG (4 x black, 4 x red)
	ST9, ST12	4-pin Molex Micro-Fit connector 43045-0426 Receptable housing: 43025-0410
	ST10, ST11	8-pin Molex Micro-Fit connector 43045-0826 Receptable housing: 43025-0810
	JB1..2, JR2_S	10-pin IDC connector (double-row)
	JB3..5	5-pin IDC connector (single-row)

*See also „3.3 Connector types in overview" on page 17.

Analog inputs on ADQ-SCU-BB

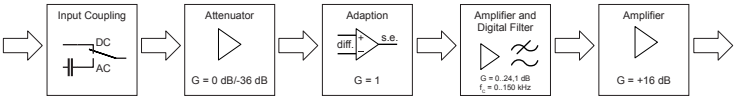
Unless otherwise specified, the specifications of the ADQ-344 are applicable.
Basically, an adjustment should be done with connected field wiring in conjunction with the ADQ-344.

Element	Condition	Specification
Channels	AI_0..31±	32 single-ended analog inputs (4 AI modules)
Resolution		18 bit ADC, the output level to the ADQ-344 is normalized to ±5.12 V
Input impedance	with attenuation	6 kΩ || 1.6 pF
	without attenuation	1 MΩ || 1.6 pF
Input coupling		AC/DC (programmable)
Input attenuation		0 dB/-35.9185 dB (programmable)
Digital filter stage	LTC1564	0..150 kHz in steps of 10 kHz programmable; 100 dB attenuation at 2.5-times cut-off frequency
Amplifier stage	LTC1564	Factor 1..16 programmable (corresponds to 0 dB..24,1 dB)
Amplifier stage	LTC1469	+16 dB (fixed)
Reasonable input voltage ranges	A = 0 dB, V = 4	0..(203 mV - 1 LSB), 1 LSB = 0.8 µV
	A = 0 dB, V = 2	0..(406 mV - 1 LSB), 1 LSB = 1.5 µV
	A = 0 dB, V = 1	0..(812 mV - 1 LSB), 1 LSB = 3 µV
	A = -36 dB, V = 4	0..(12.8 V - 1 LSB), 1 LSB = 0.05 mV
	A = -36 dB, V = 2	0..(25.6 V - 1 LSB), 1 LSB = 0.1 mV
	A = -36 dB, V = 1	0..(51.2 V - 1 LSB), 1 LSB = 0.2 mV
Slew rate	LTC1167	typ. >1.2 V/µs
	LTC1468	typ. >22 V/µs
Temperature drift	LTC1167	±4 µV/°C
	LTC1564	no manufacturer specification available
	LTC1468	±2 µV/°C
Small signal relay	Details see separate table	Type: FTR-B3CA()Z, up to 5 relays in AI signal path
Trigger inputs		4 external trigger inputs via STB8 (one per AI module)
Ground reference	Analog inputs	GND_AI
	AI trigger inputs	TRIG_AI_GND

Accuracy of the overall setup of the ADQ-SCU signal conditioning unit and the ADQ-344 multi-function DAQ and control board:

Before starting the adjustment of the AI and AO section, the measuring system should warm up for at least 30 minutes. The following measuring instruments have been used for the measurements:

- Reference voltage source: Knick J152
- 5½ digit multimeter: Siglent SDM3055
- ADQ-344 with the following settings: sample rate: 200 kHz, 5,000,000 values per channel, input range: ±5.12 V. The ADQ-344 is adjusted.



Input voltage	DC/AC	Attenuation	Adaption	Gain/Filter	Gain	Error
±10mV	DC	0 dB	G = 1	G = 16 / 20 kHz	16 dB	±0.0103%
±90mV	DC	0 dB	G = 1	G = 8 / 20 kHz	16 dB	±0.0072%
±200mV	DC	0 dB	G = 1	G = 4 / 20 kHz	16 dB	±0.0065%
±500mV	DC	0 dB	G = 1	G = 1 / 20 kHz	16 dB	±0.0065%
±1V	DC	-36 dB	G = 1	G = 8 / 20 kHz	16 dB	±0.15%
±10V	DC	-36 dB	G = 1	G = 4 / 20 kHz	16 dB	±0.08%
±19V	DC	-36 dB	G = 1	G = 1 / 20 kHz	16 dB	±0.021%

Audio monitoring stage on ADQ-SCU-BB

Element	Condition	Specification
Channels		1 x stereo audio output to connect a headphone
Digital filter stage	LTC1564	0..150 kHz in steps of 10 kHz programmable; 100 dB attenuation at 2.5-times cut-off frequency
Amplifier stage	LTC1564	Factor 1..16 programmable (corresponds to 0 dB..24,1 dB)
Output amplifier	MAX9723	0 dB..24.1 dB (programmable)
Connector	STB19	3-pin header, type: Phoenix Contact MCV 1,5/ 3-G-3,5 (Phoenix order no.: 1843237), Mating plug with push-in spring connection: Phoenix Contact FMC 1,5/ 3-STF-3,5 (Phoenix order no.: 1966101)

Analog outputs on ADQ-SCU-BB

Unless otherwise specified, the specifications of the ADQ-344 are applicable.
Basically, an adjustment should be done with connected field wiring in conjunction with the ADQ-344.

Element	Condition	Specification
Channels	AO_A..G±	8 single-ended/diff. voltage outputs; each 2 channels (AO_x/y±) are sourced by the same AO channel from the ADQ-344
Output voltage range		-20.48V..(+20.48V - 1 LSB)
Resolution		16 bit (1 LSB = 626 µV)
Offset error	not adjusted	max. 1.25 mV
Output current		max. ±10 mA per channel
Cut-off frequency		1 MHz (-3 dB)
Slew rate		min. 18 V/µs
Output impedance	output disabled	>10 MΩ
Total accuracy		2 LSB = 1.25 mV
Channel shut-down		The output channel can be shut down by suitable programming
Overload protection		On overheating of the output amplifier, the output is automatically shut down
Trigger inputs		4 external trigger inputs via STB8 (one per channel pair)
Ground reference	Analog outputs	GND_AO
	AO trigger inputs	TRIG_AO_GND

* The actual possible output rate depends strongly on the performance of your computer, the number of installed boards and the number of channels used.

Small signal relays for AI and AO section

Element	Condition	Specification
Type		FTR-B3CA()Z standard
Number	AI section	up to 5 relays in the AI signal path
	AO section	2 relays in the AO signal path
Contact type		2 x form C (DPDT)
Contact material		Gold overlay silver nickel
Contact resistance		max. 75 mΩ at 1 A/6 VDC
Switching time	Operate time	max. 3 ms
	Release time	max. 3 ms
Switching cycles	Mechanical	min. 50,000,000

Relays for auxiliary power on ADQ-SCU-BB

Element	Condition	Specification
Number/Type		8 x form C relays (SPDT), type: Finder series 34
Contact material		silver/nickel
Switching time	Operate time	max. 5 ms
	Release time	max. 3 ms
Switching cycles	Mechanical	min. 10,000,000
Switching current DC1		max. 6 A / 30 VDC (limited by Polyfuse to 4 A)
Connection	Input	STB11..14
	Output	STB15

Isolated digital inputs via ADQ-SCU-BB

Unless otherwise specified, the specifications of the ADQ-344 are applicable.

Element	Condition	Specification
Number	to ADQ-344	1 x 8 bit digital input port via STB6
Type		Isolated digital inputs (uni-directional) with Schmitt Trigger characteristic according to IEC 61131-2 (type 1)
External power supply	V_EXT_DI	15..35 VDC, typ. 24 VDC for control technology
Ground reference		GND_DI

Isolated digital outputs via ADQ-SCU-BB

Unless otherwise specified, the specifications of the ADQ-344 are applicable.

Element	Condition	Specification
Number	to ADQ-344	1 x 8 bit digital output ports via STB7
Type		Isolated digital outputs (uni-directional) according to IEC 61131-2 (type 1)
External power supply	V_EXT_DO	11..35 VDC; typ. 24 VDC for control technology
Ground reference		GND_DO

Relay board ADQ-SCU-RB

Element	Condition	Specification
TTL I/Os	PCA9698	3 x 8 bit ports (bi-directional, direction programmable for each 8 bit port)
	Inputs	Inputs can be inverted
	Outputs	Outputs programmable as sink or source drivers - Source operation max. 10 mA - Sink operation max. 25 mA
	Connection	STR5..7
Relays	Number/Type	8 form C relays (SPDT), type: Finder series 34
	Contact material	silver/nickel
	Switching time	Operation time max. 5 ms
		Release time max. 3 ms
	Switching cycles	min. 10,000,000 (mechanical)
	Switching current DC1	max. 6 A at 30 VDC
	Connection	All relay contacts (NO/NC/COM) are routed to the connectors STR1..4
	Status display	16 blue LEDs
Control	PCA9698	I^2C controlled
Ground reference		GND_PC

Powerboard ADQ-SCU-PB

Element	Condition	Specification
TTL I/Os	PCA9698	3 x 8 bit ports (bi-directional, direction programmable for each 8 bit port)
	Input	Inputs can be inverted
	Output	Outputs programmable as sink or source drivers - Source operation max. 10 mA - Sink operation max. 25 mA
	Connection	STR5..7
High-current relay	Number/Type	2 form A (SPST), type: Finder series 67 (power relay)
	Contact material	$AgSnO_2$
	Switching time	Operation time max. 25 ms
		Release time max. 5 ms
	Switching cycles	min. 1,000,000 (mechanical)
	Switching current DC1	Each relay has 2 closing contacts switching in parallel: max. 2 x 50 A/ 24 VDC
	Connection	Single-pole high current connector of type: Würth Electronic REDCUBE Direct Plug Terminal WP-PLUG
	Relay 1 switch path	ST1 to ST5 (ground run through from ST2 to ST6)
	Relay 2 switch path	ST4 auf ST8 (ground run through from ST3 to ST7)
	Sense lines	Signal at the relay input (U1_IN/U2_IN) can be measured via ST9
	Status display	2 blue LEDs
Standard relay	Number/Type	4 form A relays (SPST), type: Finder series 34
	Contact material	silver/nickel
	Switching time	Operation time max. 5 ms
		Release time max. 3 ms
	Switching cycles	min. 10,000,000 (mechanical)
	Switching current DC1	max. 6 A / 30 VDC, here max. 5 A due to the maximum current of the power measurement via LTC2945
	Connection	Input (U_IN) via ST10, outputs (U3..6_OUT) via ST11
	Sense line	Signal at the relay input (U_IN) can be measured via ST12
	Status display	4 blue LEDs
Power measurement	Channels	4 channels U3..6
	Current measurement	20 mΩ shunt per relay input, measurement range 0..5 A
	Voltage measurement	at the relay input (U_IN), measurement range 0..30 VDC
Control	Relays	I^2C controlled via PCF8574
	Powermeter	I^2C controlled, 4 x LTC2945
Ground reference		GND_PC

Counter

Element	Condition	Specification
Counter type		32 bit down-counter
Preset		32 bit start value can be loaded
Mode		Counting downwards to zero (retriggerable) or continuously counting with automatic reload of the start value
Threshold value	Schwellwert < Preset	Programmable threshold value which can generate an interrupt on match with the current counter value
Strobe	Strobe < Preset	Pulse duration programmable in steps of 15.15 ns
Interrupt		On zero axis crossing or on reaching the threshold value
Inputs	via HDMI (STB18)	Enable input (CNT_EN) External trigger input (CNT_TRIG) External clock input (CNT_EXT_CLK)
Outputs	via HDMI (STB18)	Strobe output (CNT_OUT)

I^2C bus

Element	Condition	Specification
Modes		Fast Mode (Fm): 0.4 Mbit/s
Bus subscribers		Max. 128 devices can be addressed in slave mode; ADQ-SCU is always slave!
Bus signals	via HDMI (STB18)	Clock line "Serial Clock" (I2C_SCL) Data line "Serial Data" (I2C_SDA)
Address format		7 bit slave address + read/write bit as LSB
Data format		Up to 4 data bytes can be transferred per write or read cycle
Isolation	via opto-coupler (type: ISO1541)	For bus subscribers on base board (incl. temperature sensor and EEPROM), power board and relay board

Incremental encoder (in preparation, all details without guarantee)

Element	Condition	Specification
Counter type		16 bit up/down counter + direction
Quadrature signal		A/B channel with 90° phase shift
Coding		Gray code
Resolution		4-times per signal period ("each edge counts")
Error correction		Suppression of invalid states on hardware level
Pulse frequency sensor		max. 33 MHz
Reset input		asynchronous reset, setzt Zähler auf 0000 Hex
Interrupt		Interrupt on exceeding the counting range
Inputs	via STB10	Sensor input "Channel A" (INC_A) Sensor input "Channel B" (INC_B) External reset input (INC_EXT_RST)

Frequency measurement

Element	Condition	Specification
Measurement range	Frequency (period)	f_{IN} = 0.0153 Hz (T_{IN} = 65 s) up to f_{IN} = 660 kHz (T_{IN} = 1.5 µs)
	Pulse duration (high)	T_{ON} in steps of 15.15 ns
Resolution	Period & pulse	15.15 ns
Accuracy	system dependent	±15.15 ns
Input	via HDMI (STB18)	Frequency measurement input (FRQ_IN)

PWM output

Element	Condition	Specification
Rectangular signal output	Frequenz (Periode)	f_{OUT} = 0.0153 Hz (T_{OUT} = 65 s) up to f_{OUT} = 660 kHz (T_{OUT} = 1.5 µs).
	Impulsdauer (High)	T_{ON} in steps of 15.15 ns; T_{ONmax} = T_{OUT} - 15.15 ns
Duty factor	Period/pulse duration	Min. 1% steps or better (slow frequencies can be resolved more accurately than high frequencies)
Resolution	Period & pulse	15.15 ns
Input	via HDMI (STB18)	Enable input (PWM_EN)
Output	via HDMI (STB18)	PWM output (PWM_OUT), can be inverted by software

6. Appendix

6.1 Accessories

6.1.1 Cables

- **ADQ-CR-VHDCI-68M/68M-1,2m** (Art.-Nr. 150597)
  Double-shielded round cable from 68-pin VHDCI male connector to 68-pin VHDCI male connector, twisted pair lines, length: ca. 1.2 m
- **ADQ-CR-VHDCI-68M/68M-1,8m** (Art.-Nr. 146813)
  Double-shielded round cable from 68-pin VHDCI male connector to 68-pin VHDCI male connector, twisted pair lines, length: ca. 1.8 m
- **ADQ-CR-HDMI-MM-1m** (Art.-Nr. 127015)
  HDMI cable for connection of the digital I/Os and trigger signals with the special terminal block, length: 1 m

6.2 Manufacturer and support

ALLNET® and ALLDAQ® are registered trademarks of the ALLNET® GmbH Computersysteme. For questions, problems and product information please contact the manufacturer directly:

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6.3 Important notes

6.3.1 Packaging ordinance

Basically manufacturer and distributors are committed to take care, that sales packaging are withdrawn after use from the end user and applied to a new disposal or to a material recycling as a matter of principle (translated according to § 4 sentence 1 of VerpackVO). If you have problems as customer on disposal of packaging and shipping material please write an email to info@allnet.de.

6.3.2 Recycling note and RoHS compliance

Please note, that parts of products of ALLNET® GmbH should be disposed in recycling centers resp. may not be disposed via the household waste (printed circuit boards, power adapters and so on).

ALLNET® products are manufactured in accordance with RoHS (RoHS = Restriction of the use of certain hazardous substances).

6.3.3 Warranty

Within the warranty time we eliminate manufacturing and material defects free of charge. The warranty terms valid for your country can be found on the homepage of your distributor. If you have questions or problems applying the warranty you can contact us during our normal opening hours under the following phone number +49 (0)89 894 222 – 474 or by email: support@alldaq.com.

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