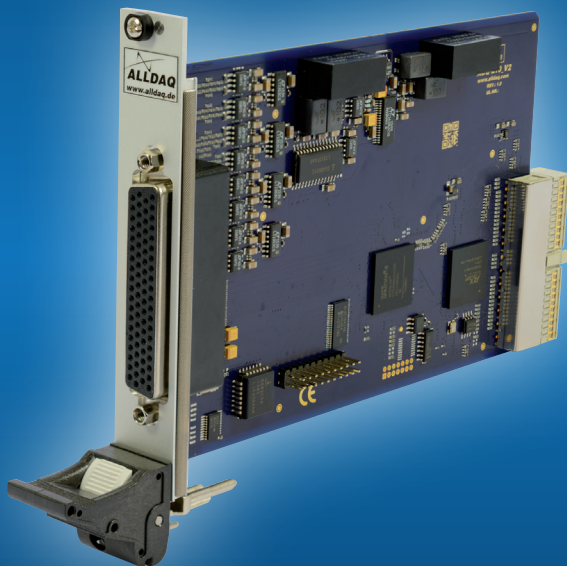




Manual

Rev. 2.0 EN



ADQ-210 cPCI

Multi I/O board with 16 analog inputs up to 500 kHz,
32 digital I/Os, 3 x 16 bit counter

Imprint

Manual ADQ-210 series
Rev. 2.0
Date: 03/27/2017

Manufacturer and Support

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All information contained in this manual has been reviewed with great care. Nevertheless errors cannot be eliminated completely. Specifications and the content of this manual are subject to change without notice.

We are appreciated for notification of possible errors.

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Table of Content

1. Introduction	5
1.1 Scope of delivery	5
1.2 Safety instructions	5
1.3 Location of installation and mounting	6
1.4 Short description	6
1.5 System requirements	7
1.5.1 Hardware	7
1.5.2 Software	7
2. Initial operation	9
2.1 Installing the board	9
2.2 Software installation	9
2.2.1 Installation under Windows	9
2.3 Test programm	9
2.4 ALLDAQ-Manager	10
2.5 Adjustment/Calibration	11
2.5.1 Factory adjustment	11
2.5.2 User adjustment	11
2.5.3 DAkKS calibration	11
3. Functional groups	13
3.1 Block diagram	13
3.2 Analog inputs	14
3.2.1 Nyquist-Shannon sampling theorem (Oversampling)	14
3.2.2 Wiring	15
3.2.2.1 Differential inputs	15
3.2.2.2 External trigger A/D section	16
3.2.3 Programming	16
3.2.3.1 Single value acquisition	16
3.2.3.2 Timer-controlled acquisition	16
3.3 Bi-directional digital I/Os	18
3.3.1 Wiring	18
3.3.2 Programming	19
3.3.2.1 Simple input/output	19
3.3.2.2 Streaming Operation	19

3.4 Counter	20
3.4.1 Wiring	20
3.4.1.1 Standard versions (ADQ-212/215)	20
3.4.1.2 OEM versions	21
3.4.1.3 External wiring for variable duty-cycle (PWM)	22
3.4.2 Programming	23
3.4.2.1 Standard operation modes	23
3.5 External interrupt	23
3.5.1 Wiring	23
3.5.2 Programming	23
4. Appendix	25
4.1 Specifications	25
4.2 Pinouts	29
4.2.1 78-pin D-Sub female connector (ST1) ADQ-212/215	29
4.2.2 25-pin D-Sub connector (ST2)	30
4.3 Accessories	32
4.4 Manufacturer and support	32
4.5 Important notes	33
4.5.1 Packaging ordinance	33
4.5.2 Recycling note and RoHS compliance	33
4.5.3 CE certification	33
4.5.4 Warranty	33

1. Introduction

Please check the box and the content for damages and completeness before taking the device into operation. If any fault should be detected please inform us immediately.

- Shows the packing some evidence to damaging during transport?
- Any traces of use to be recognized at the device?

The device may not be taken into operation if it is damaged. In case of doubt please contact our technical service department.

Please read – before installing the device – this manual watchfully!

Note for OEM version:

Unless otherwise specified the OEM version corresponds with the ADQ-212.

1.1 Scope of delivery

- ALLDAQ ADQ-212-cPCI, ADQ-215-cPCI or the OEM version
- 78-pin D-Sub male connector
- 25-pin D-Sub male connector
- Additional mounting bracket/bezel with 25-pin D-Sub female connector to 20-pin IDC connector for cPCI (ADQ-AP-D25F-cPCI)
- Driver software and documentation under: www.alldaq.com/downloads

1.2 Safety instructions



Necessarily note the following advices:

- Necessarily avoid touching of cables and connectors inside the PC with the board.
- Never expose the device to direct solar radiation during operation.
- Never run the device near heat sources.
- Protect the device before humidity, dust, liquids and fumes.
- Don't use the device in damp rooms and never in explosive areas.
- A repair may only be done by trained and authorized persons.



- Please note before initial operation of the device especially when using voltages greater 42 V the installation rules and all relevant standards (including VDE standards).
- We recommend to tie all unused inputs basically to the corresponding reference ground to avoid cross talk between the input lines.
- Before connecting or removing cables with your board always disconnect your field wiring from the power supply.



- Ensure that no static discharge can occur passing the board when handling it. Follow the standard ESD safety precautions (see also chapter 2.1 on page 9).
- Never connect devices with voltage-carrying parts, especially not with mains voltage.
- The user must take appropriate precautions to avoid unforeseeable misuse.

For damages caused by improper use and subsequent damages any liability by ALLNET® GmbH is excluded.

1.3 Location of installation and mounting

The PC boards of the ADQ-210 series are digital I/O boards for industrial use. Depending on the version the models of the ADQ-210 series are...

... for installation into a free CompactPCI slot (ADQ-21x-cPCI).

PC boards may not be taken into operation outside of appropriate PC systems. For the order of operation on installing the devices please read the chapter „Initial operation“ in this manual and the documentation of your PC.

The ADQ-210 series may only be used in dry rooms. PC boards are not for use with tough environment conditions (e.g. outside). Ensure a very good ventilation. Take care for proper fitting of the connection cables. Installation has to be done in a way that the cables (PC connection and field wiring) are not in tension else they could release itself.

1.4 Short description

The PC plug-in boards of the ALLDAQ ADQ-210 series are **universal multi I/O boards for standard measuring and control tasks in laboratory, test bay and quality assurance**. The CompactPCI boards offer 16 differential analog inputs with a total sample rate of up to **500 kHz at 16 bit** resolution. Depending on model you have the input voltage ranges $\pm 20V$ (ADQ-212) or $\pm 50V$ (ADQ-215) available. See also Table 1 on page 14.

Overall the ADQ-210 series comes with **32 bi-directional digital I/Os** whose direction can be programmed by port (8 bit). Therefrom 16 digital I/Os are provided by the 78-pin D-Sub female connector at the mounting bracket of the board and further 16 digital I/Os can be used by an additional mounting bracket (included). The voltage level of all digital I/Os can be switched between +3.3V and +5V in common by software. Each output can drive up to 24 mA.

As a counter the established **standard counter chip of type 8254 with three 16 bit counter** is used. Each counter can be programmed separately. Cascading can be realized by an appropriate external wiring, e.g. for output of a signal with a variable duty cycle. As a clock source an external rectangular signal with max. 10 MHz must be provided.

Note for OEM version:

The OEM version provides an on-board crystal oscillator sourcing the clock input CLK_0 with 10 MHz. The counter outputs OUT_2..0 are of open collector type.

1.5 System requirements

1.5.1 Hardware

- PC system with a current Intel® or compatible processor based on the x86(-64) architecture
- A free CompactPCI slot with 4 HP width

1.5.2 Software

System Driver

- Windows Vista (SP2) (32 and 64 bit)
- Windows 7 (32 and 64 bit)
- Windows 8/8.1 (32 and 64 bit)
- Windows 10 (32 and 64 bit)

ALLDAQ-Manager

By the ALLDAQ-Manager you have central access to the software developer kit (SDK), several utility programs and help files. The ALLDAQ-Manager can be found in the info area of the taskbar (usually at the bottom right corner of the desktop) or by the Windows Start menu. See also chapter on page 11.

Software Developer Kit (SDK)

A function library (API) with example code for high-level language programming is included. Please note the corresponding help file included with the SDK.

LabVIEW Support

A library with virtual instruments (VIs) for easy access to the ALLDAQ hardware is included with the ALLDAQ SDK.

MATLAB Support

An adapted MATLAB® interface for the ALLDAQ hardware with examples and a help file is included with the ALLDAQ SDK.

2. Initial operation

2.1 Installing the board

Please read the manual of your computer prior installing the board regarding the installation of additional hardware components.

Handling the board should be done with care to ensure that the device will not be damaged by electrostatic discharge (ESD), mechanical stress or current surges. Ensure to take all safety precautions to avoid an electric shock and follow the standard ESD safety precautions.

Follow this order of operation:

- Unplug the mains plug of your PC system.
- Open the housing as described in the manual of your PC system.
- Make sure that electrostatic discharge cannot occur via the board when you plug it in. At least one hand should be grounded in order to dissipate any static charge.
- Push the plug-in board carefully and with only a little force into the appropriate slot. Check that the board is not cant and fully plugged in.
- If you want to use the additional mounting bracket for the TTL digital I/Os choose two slots side by side for installation. Remove (if necessary) an additional blind bracket for the slot.
- Screw all mounting brackets.
- Close the housing as described in the manual of your PC system



2.2 Software installation

2.2.1 Installation under Windows

Run the file *ALLDAQDriverSetup32.exe* for 32bit systems resp. *ALLDAQDriverSetup64.exe* for 64bit systems in the target directory of your download. After successful installation the ALLDAQ-Manager can be found in the info area of the taskbar (usually at the bottom right corner) and in the Windows Start menu. By the ALLDAQ-Manager you have access to the software developer kit (SDK), several utility programs and help files.

2.3 Test programm

Simple test programs can be found in the ALLDAQ-SDK. For each programming language a sub-directory „Applications“ can be found with test programs for your ALLDAQ hardware.

With the ALLDAQ-Manager you can retrieve several information of the installed ADQ hardware.

2.4 ALLDAQ-Manager

The ALLDAQ-Manager under Windows gives you a quick overview of the parameters of the ADQ driver system and offers a central access to software tools and help files. You can find the ALLDAQ-Manager in the info area of the taskbar (as a rule at the bottom right) or via the Windows start menu.

ALLDAQ-Manager in overview:

- Information on the installed ALLDAQ hardware in overview
- XML export of the driver configuration for archiving and support
- Tool for interactive illustration of the pin-assignment with the possibility to generate a PDF
- Tool for user calibration
- Convenient access to the software developer kit (SDK) for high-level language programming with examples and simple test programs
- Quick access to the help files (*.chm)

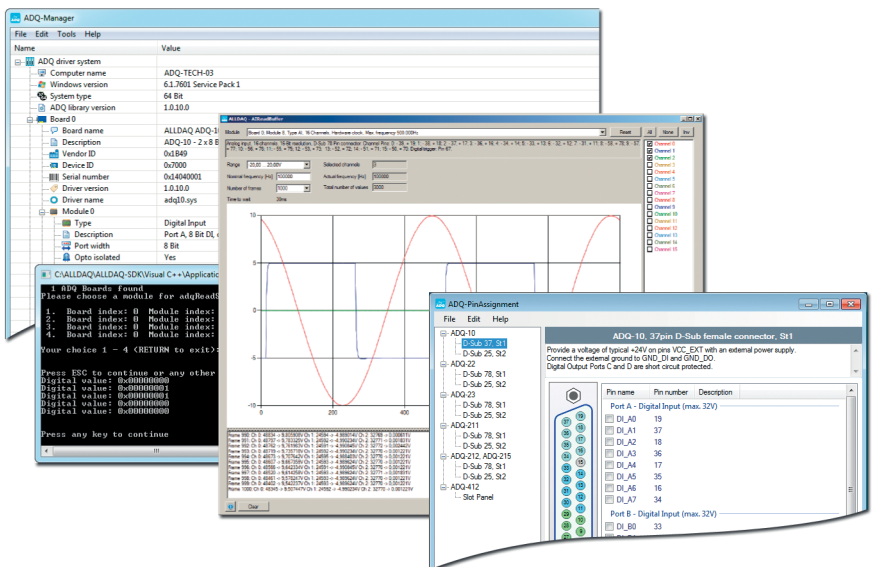


Figure 1: ALLDAQ-Manager and SDK programs

2.5 Adjustment/Calibration

By the ALLDAQ-Manager you can select which adjustment data record (factory or user adjustment) should be activated when booting the computer. You can change the setting via the ALLDAQ-Manager.

2.5.1 Factory adjustment

The ADQ-210 series will be adjusted before delivery. The adjustment data will be stored into an EEPROM. If a re-adjustment should be necessary please contact our service department. For contact details see chapter on page 33.

2.5.2 User adjustment

For a precise voltage measurement considering multiple error factors, e.g. caused by the field wiring you can adjust the analog inputs by yourself. After adjustment the application-specific adjustment data can be stored beside the factory adjustment data into an EEPROM.

Please follow the procedure below:

1. Power-on the system with the ADQ-210 series.
2. Connect the part of the field wiring you want to include into the adjustment.
3. Apply a constant voltage to one channel after the other and monitor the voltage by a high-precision voltmeter (e.g. multimeter). Make sure, that the voltmeter has a higher accuracy than the accuracy of your board. See also Figure 2.
4. Run the calibration tool in the ALLDAQ-Manager under "Tools - Calibration" and follow the procedure in the appropriate help file. See also chapter 2.4 on page 10.

TIP: To achieve the best accuracy, we recommend to set that sample rate which one you want to use in your measurement later.

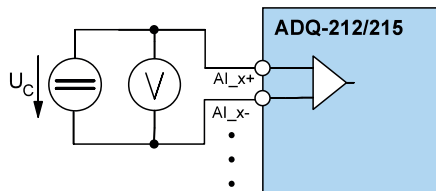


Figure 2: Wiring for calibration

2.5.3 DAkkS calibration

We collaborate with independent test laboratories accredited by the Deutsche Akkreditierungsstelle GmbH (DAkkS). On-demand please contact our service department. For contact details see chapter 4.4 on page 32.

3. Functional groups

3.1 Block diagram

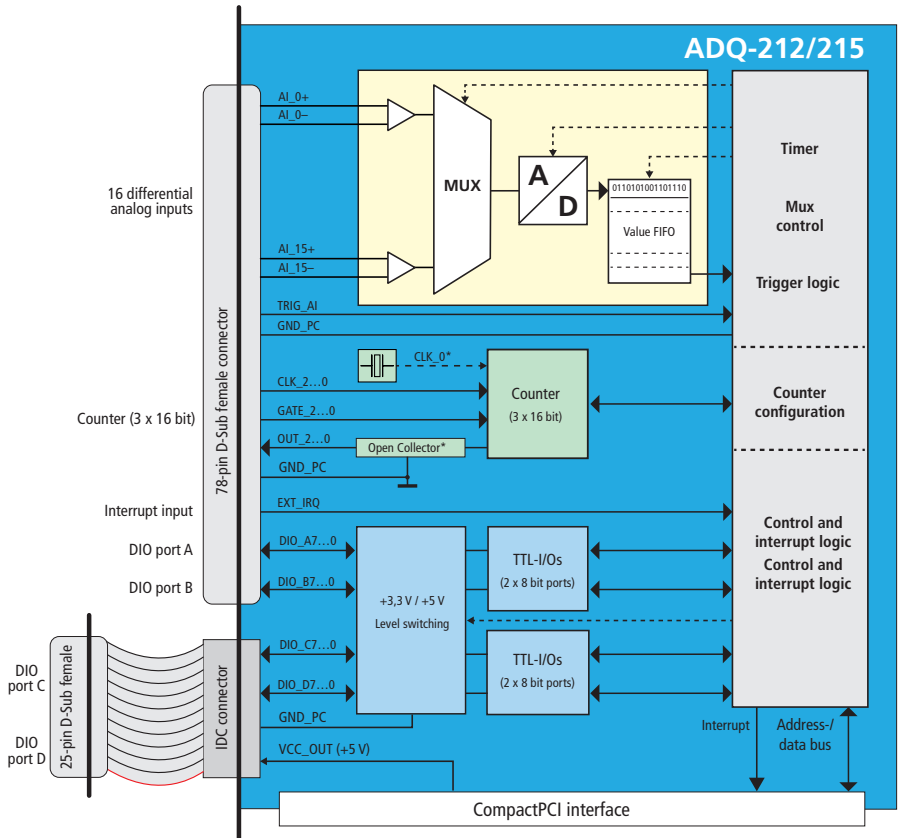


Figure 3: Block diagram ADQ-212/215

- 16 differential analog inputs
- 16 bi-directional TTL digital I/Os (2 x 8 bit ports) at the 78-pin D-Sub female connector
- 16 bi-directional TTL digital I/Os (2 x 8 bit ports) can be used by an additional mounting bracket on demand (included)
- 3 x 16 bit counter (type: 8254)*
- 1 x external interrupt input

* The OEM version sources the clock input CLK_0 with a 10MHz on-board crystal oscillator (in this case pin 63 is not connected). The counter outputs OUT_2..0 are of open collector type.

3.2 Analog inputs

The models ADQ-212 and ADQ-215 provide 16 differential input channels. All channels are scanned sequentially, i. e. if you scan all channels the maximum sample rate per channel calculates as follows: 500 kHz / 16 channels = 31.25 kHz. All models are decoupled by a high-impedance input buffer. The input impedance differs depending on model (see Table 1).

Input characteristics of the ADQ-210 series in overview:

	ADQ-212 (OEM)	ADQ-215
Channels	16 differential	16 differential
Bandwidth (rectangular)	3 kHz	2 kHz
Resolution	16 bit	16 bit
Total sample rate	500 kHz	500 kHz
Input range U_{AI}	-20.000000...19.999390 V	-50.000000...49.998474 V
Input impedance	20 M Ω	80 M Ω

Table 1: Input characteristics

The input voltage range is defined by the hardware and depends on model.



Note, that the maximum voltage at the analog inputs must not exceed the input voltage range of the particular model by more than 5 V $\pm(U_{AI} + 5V)$. Otherwise the board can be damaged irreversibly.

3.2.1 Nyquist-Shannon sampling theorem (Oversampling)

The Nyquist-Shannon sampling theorem tells us, that the sample rate for a periodic signal, whose maximum frequency component should be f_{Pmax} , must be at least twice as high, i. e. $2 \cdot f_{Pmax}$ or higher.

In practice we recommend to choose a sampling rate by the factor 5 or 10 higher than f_{Pmax} to replicate the signal form truly. This issue is also called "oversampling".

Example:

The max. frequency component f_{Pmax} . ($1/t_p$) of the signal frequency should be 50 kHz. The sample rate f_s ($1/t_s$) should be at least $5 \times 50 \text{ kHz} = 250 \text{ kHz}$.

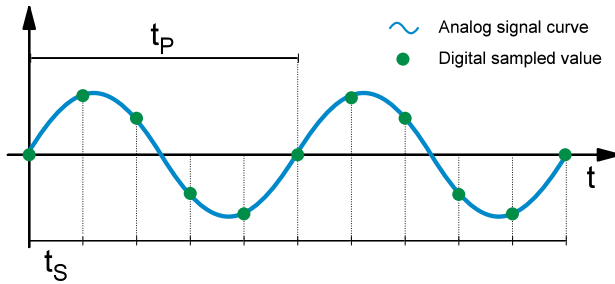


Figure 4: Nyquist-Shannon sampling theorem

3.2.2 Wiring

Basically we recommend using of high-quality shielded cables.

3.2.2.1 Differential inputs

In ideal case a differential input measures only the potential difference between the positive and the negative input. By this common mode interferences will be largely suppressed. This is very favourably for acquisition of signals without common ground reference, to suppress ground loops and generally in noisy environments. The input voltage range is defined by the hardware and differs depending on the model. For the differential voltage U_{AI_X} applies: $U_{AI_X} = (U_{AI_X+}) - (U_{AI_X-})$, i. e. the absolute value of the potential difference between AI_X+ and AI_X- may be 20 V max. for the ADQ-212 resp. 50 V for the ADQ-215.

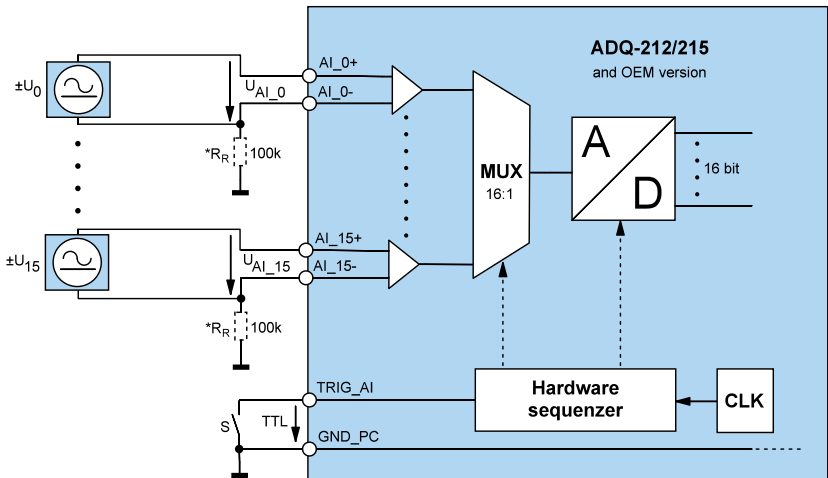


Figure 5: Differential inputs

***TIP:** We recommend to connect each differential input with PC ground by a reference resistor R_R (100 k Ω recommended) as shown in Figure 5.

3.2.2.2 External trigger A/D section

All models of the ADQ-210 series provide a digital trigger input for the A/D section. Depending on configuration the conversion can be started by a rising, a falling or any of both edges.

The digital trigger input (TRIG_AI, pin 67) is designed for a TTL high-level of +5V. The trigger signal requires a reference to PC ground (GND_PC).

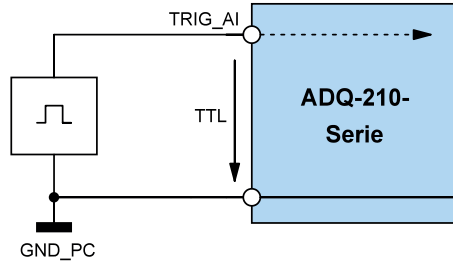


Figure 6: Wiring digital trigger A/D section

3.2.3 Programming

For programming the analog acquisition there is a differentiation between the so-called "Single value acquisition" and the "Timer-controlled acquisition".

3.2.3.1 Single value acquisition

This operation mode is for acquiring single values without fixed time reference.

Depending on configuration the conversion can be started by software or by a rising, falling or any edge at the external trigger input (TRIG_AI).

Please note the order of operation as described in the online help.

3.2.3.2 Timer-controlled acquisition

With the timer-controlled acquisition you can sample signals in defined time intervals. You can acquire a pre-defined number of frames or continuously. The so-called A/D value FIFO is a fast buffer memory to enable a continuous data transfer to the PC. The channel multiplexer are controlled by channel-list, which can include 16 entries maximum.

Depending on configuration the conversion can be started by software or by a rising, falling or any edge at the external trigger input (TRIG_AI).

Please note the order of operation as described in the online help.

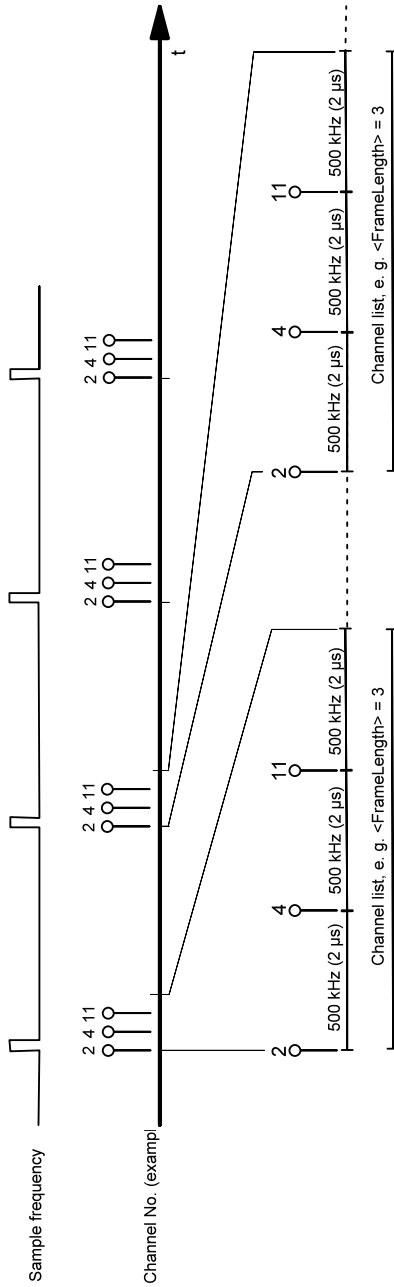


Figure 7: Timer-controlled acquisition

In dependency of the number of channels used the max. sample rate is calculated as follows:

Number of channels	max. sample rate/channel	Number of channels	max. sample rate/channel
1	500 kS/s	9	55.55 kS/s
2	250 kS/s	10	max. 50 kS/s
3	166.66 kS/s	11	max. 45.54 kS/s
4	125 kS/s	12	max. 41.66 kS/s
5	100 kS/s	13	max. 38.46 kS/s
6	83.33 kS/s	14	max. 35.71 kS/s
7	71.43 kS/s	15	max. 33.33 kS/s
8	62.5 kS/s	16	max. 31.25 kS/s

Table 2: Maximum sample rate per channel

3.3 Bi-directional digital I/Os

The ADQ-210 series provides four bi-directional 8 bit wide digital I/O ports. 2 of the ports (DIO_Ax and DIO_Bx) can be attached by the 78-pin D-Sub female connector at the mounting bracket of the board itself, 2 more ports (DIO_Cx and DIO_Dx) can be used on demand by an additional 25-pin D-Sub female connector. An additional front bezel for cPCI slots (ADQ-AP-D25F-cPCI) is included (see pinout on page 30).

The voltage level of all digital I/Os can be switched between +3.3V and +5V in common by software. Each output can drive up to 24 mA.

Note: After power-up all ports are configured as input.

3.3.1 Wiring

When wiring the inputs and outputs take care that the TTL level is met (see specifications on page 27) and that a reference to PC ground (GND_PC) must be established. The max. output current is $I_O = I_{OL} = I_{OH} = 24\text{ mA}$.

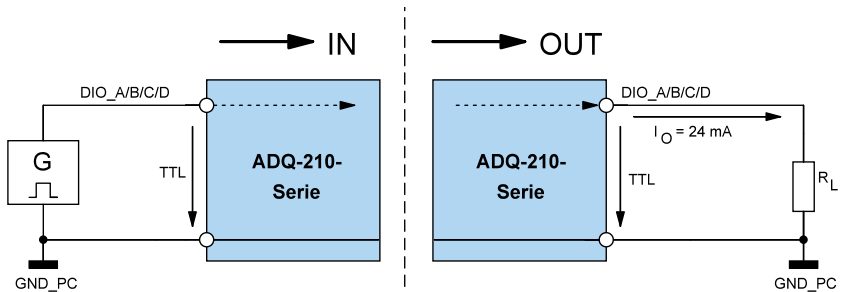


Figure 8: Wiring of the digital I/Os

3.3.2 Programming

The four digital I/O ports (DIO_Ax, DIO_Bx, DIO_Cx, DIO_Dx) can be programmed port-wise (8 bit wide) as input or output. After power-up all bi-directional ports are configured as input.

3.3.2.1 Simple input/output

In this operation mode one digital value of the appropriate port can be read resp. output. The port direction is defined by software.

Note: A port configured as output can be read back also!

Follow the order of operation as described in the online help.

3.3.2.2 Streaming Operation

The software-controlled streaming operation enables a continuous reading of digital inputs resp. the output of a bit pattern stream depending on the port direction with up to 1 kS/s.

Follow the order of operation as described in the online help.

3.4 Counter

As counter the well-proven standard counter chip of type 8254 with **three 16 bit counter** is used. Each counter can be programmed separately. Cascading the counter, e.g. for output of a signal with a variable duty-cycle, can be realized by an appropriate external wiring. The clock must be provided by an external rectangular signal with max. 10 MHz. With the OEM version a 10 MHz crystal oscillator is on-board sourcing the clock input CLK_0.

3.4.1 Wiring

Please note the different wiring of the counter outputs from standard and OEM versions as well as the sourcing of CLK_0 by an on-board crystal oscillator on the OEM version.

3.4.1.1 Standard versions (ADQ-212/215)

The counter inputs and outputs are designed for TTL level and need a reference to PC ground (GND_PC). The max. output current at low-level is $I_{OL} = 7,8\text{mA}$ and at high-level $I_{OH} = 6\text{mA}$.

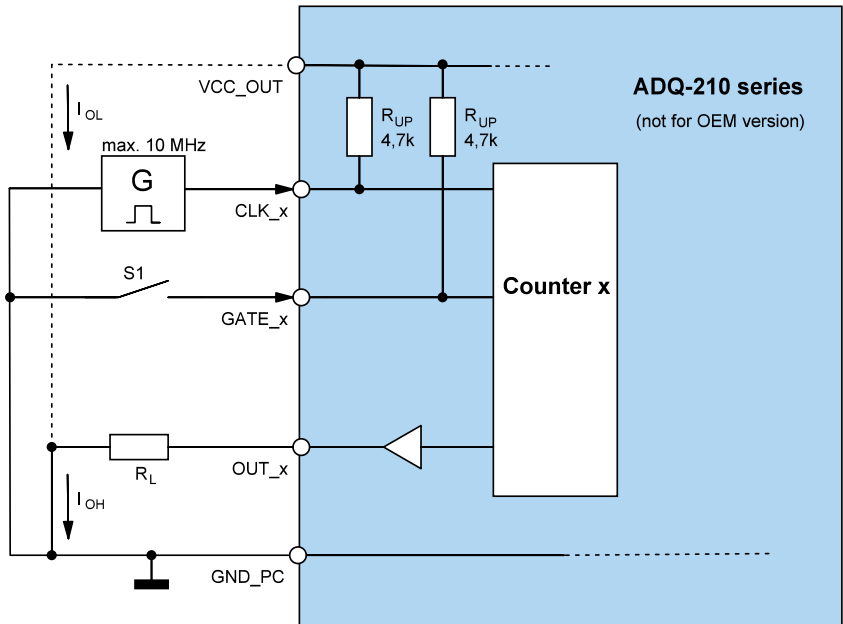


Figure 9: Wiring of the TTL counter I/Os

3.4.1.2 OEM versions

On the OEM version the counter outputs (OUT_0..2) are designed as open-collector outputs. This enables you to control external signals directly e. g. in industrial process and control where typically 24 V are used. As soon as the output is conductive (logical "1") the R_L will be switched against ground. A logical "0" means the output is in a high-impedance state so that no current I_O flows.



Note: the following limits may not be exceeded. Compliance has to be checked for each channel separately.

- Output current $I_O = U_{EXT} / R_L = \text{max. } 30 \text{ mA}$
- External voltage U_{EXT} max. 42 V
- Power loss $P_O = I_O \cdot U_O = \text{max. } 85 \text{ mW}$
- $R_L = \text{min. } 330 \Omega, \text{ max. } 4 \text{ k}\Omega$
- $U_{OL} = \text{typ. } 0.35 \text{ V, max. } 0.6 \text{ V}$

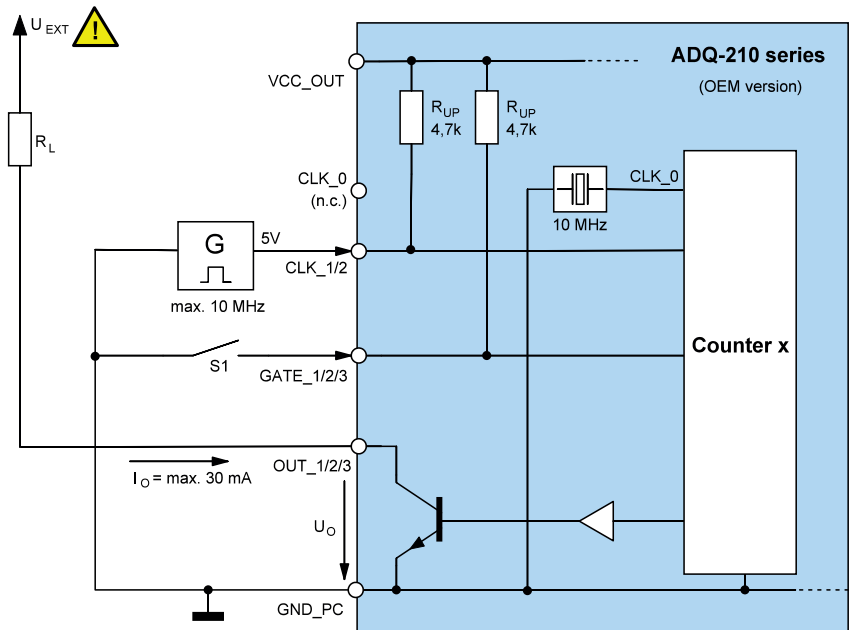


Figure 10: Counter with open-collector outputs

The counter inputs are designed for TTL level. The counter inputs as well as the counter outputs need a with a ground reference to PC ground (GND_PC). Also the ground of the counter outputs refers to PC ground (GND_PC).

3.4.1.3 External wiring for variable duty-cycle (PWM)

A special use case for the counter is the output of a rectangular signal with variable duty-cycle – often called pulse width modulation – however this is misleading because there happens no real modulation. With an appropriate external wiring of the counter 0...2 you can output a rectangular signal with variable duty-cycle. The duty-cycle can be set between 1...99% in steps of 1%. Counter 0 (prescaler) must be sourced at CLK_0 by an external clock of max. 10 MHz. The result is a max. frequency for the output signal of 50 kHz.

The frequency f_{OUT_2} is calculated as follows:

$$f_{OUT_2} = \frac{\text{External clock}}{\text{Prescaler} \cdot 100} \quad (\text{with prescaler} = 2 \cdot (2^{16} - 1))$$

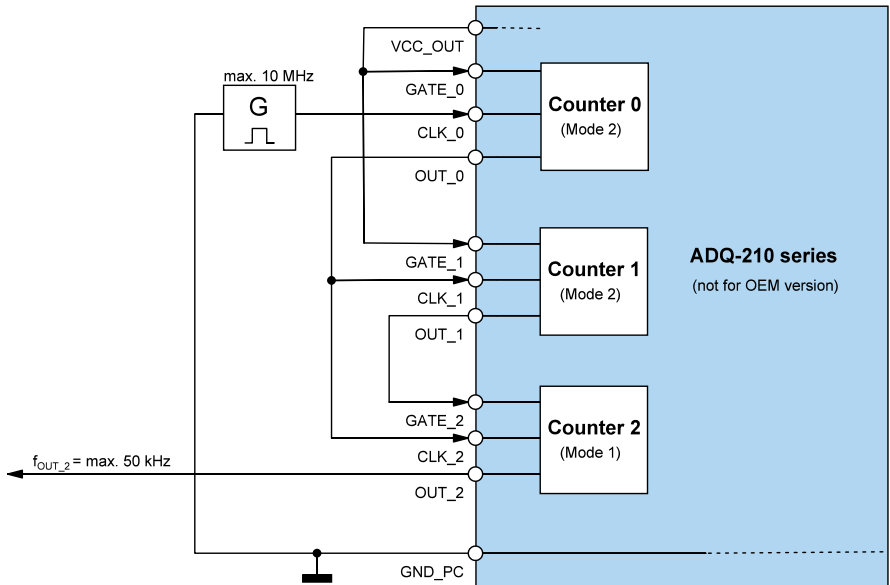


Figure 11: Wiring for variable duty-cycle (standard versions)

Note:

For wiring the counter outputs of the OEM version please contact our support department under: support@allda.com.

3.4.2 Programming

The counter chip of type 82C54 provides three 16bit counter which can be configured separately.

Please note the order of operation as described in the online help.

3.4.2.1 Standard operation modes

Each of the counter can be configured independently for one of the following operation modes:

- Mode 0: Change of state on zero axis crossing
- Mode 1: Re-triggerable „One shot“
- Mode 2: Asymmetric divider
- Mode 3: Symmetric divider
- Mode 4: Counter start by software trigger
- Mode 5: Counter start by hardware trigger

For programming please note the order of operation as described in the online help.

3.5 External interrupt

3.5.1 Wiring

The external interrupt input (EXT_IRQ, pin 48) is designed for a TTL high-level of +5V. The interrupt signal requires a reference to PC ground (GND_PC).

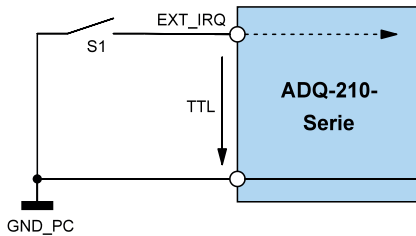


Figure 12: Wiring of the external interrupt input

3.5.2 Programming

By appropriate programming the external interrupt can be enabled for rising, falling or any of both edges. As soon as an interrupt occurs, it is sent directly to the PC.

Please note the order of operation as described in the online help.

4. Appendix

4.1 Specifications

Analog inputs

Condition: $T_A = 25^\circ\text{C}$

Element	Condition	Specification
Channels	ADQ-212/215	16 differential
A/D converter		500 kHz, 16 bit
Bandwidth (rectangular)	ADQ-212	3 kHz
	ADQ-215	2 kHz
Input voltage range	ADQ-212	-20.000000...19.999390 V (1LSB = 610 μV)
	ADQ-215	-50.000000...49.998474 V (1LSB = 1.5 mV)
Over-voltage protection	ADQ-212	-25 V...+25 V
	ADQ-215	-55 V...+55 V
Total accuracy	ADQ-212	typ. 0.01%, typ. 0.1% at fullscale
	ADQ-215	tbd.
Input impedance	ADQ-212	20 M Ω
	ADQ-215	80 M Ω
Value FIFO		8192 values
Channel list	channel selection	16 entries
Total sampling frequency	Streaming operation	max. 500 kHz (2 μs)
Sample frequency/ channel	depends on number of channels	1 channel: max. 500 kHz, min. ~ 0.008 Hz 16 channels: max. 31.25 kHz, min. ~ 0.008 Hz
Sample time range		2 μs to ~ 130 s (in steps of 30.30 ns)
Trigger modes	Start	Software, digital trigger input
	Stop	Software, digital trigger input
Ext. trigger edges		rising, falling, any
Ext. digital trigger	Pin 67 (TRIG_AI)	+5V TTL input (see also digital-I/Os)
Ground reference		GND_PC

Accuracy of the ADQ-212 analog inputs

Conditions: 100 values sampled at 100 kHz and subsequent averaging.

Measurement range	Data point	Measurement uncertainty (regarding data point)	Standard deviation (coverage factor $k = 2$)
$\pm 20\text{ V}$ range (1 LSB = $610\ \mu\text{V}$)	15 V	max. $\pm 2.44\ \text{mV}$ ($\pm 0.016\%$)	$\pm 1.63\ \text{mV}$
	10 V	max. $\pm 1.83\ \text{mV}$ ($\pm 0.018\%$)	$\pm 1.41\ \text{mV}$
	1 V	max. $\pm 2.69\ \text{mV}$ ($\pm 0.269\%$)	$\pm 1.46\ \text{mV}$

Accuracy of the ADQ-215 analog inputs

Conditions: 100 values sampled at 100 kHz and subsequent averaging.

Measurement range	Data point	Measurement uncertainty (regarding data point)	Standard deviation (coverage factor $k = 2$)
$\pm 20\text{ V}$ range (1 LSB = $1.5\ \text{mV}$)	50 V	tbd.	tbd.
	10 V	tbd.	tbd.
	1 V	tbd.	tbd.

Bi-directional digital I/Os (TTL)Condition: $T_A = 25^\circ\text{C}$

Element	Condition	Specification
Channels		2 x 8 bit digital input/output ports
Type		bi-directional (direction port-wise configurable by software)
Level changeover		+3.3 V/5 V (switchable for all ports in common by software)
U_{IH}	VCC = 5V	min. 2.0V
U_{IH}	VCC = 5V	max. 0.8V
I_I		typ. $\pm 1 \mu\text{A}$
U_{OH}	$I_O = -24 \text{ mA}$	min. 2.4V
U_{OL}	$I_O = 24 \text{ mA}$	max. 0.5V
I_O	per channel	$\pm 24 \text{ mA}$
Streaming operation	per port	max. 1 kS/s (via software timer)
Ground reference		PC ground (GND_PC)

CounterCondition: $T_A = 25^\circ\text{C}$

Element	Condition	Specification
Number		3 x 16 bit
Type		8254
Clock source	Standard versions	external source, max. 10 MHz
	OEM version	10 MHz crystal oscillator on-board
Operation modes	programmable by software	Mode 0: Change of state on zero axis crossing Mode 1: Re-triggerable „One shot“ Mode 2: Asymmetric divider Mode 3: Symmetric divider Mode 4: Counter start by software trigger Mode 5: Counter start by hardware trigger
U_{IH} (CLK_x, GATE_x)	VCC = 5V	min. 2.0V
U_{IL} (CLK_x, GATE_x)	VCC = 5V	max. 0.8V
I_I (CLK_x, GATE_x)		typ. $\pm 1 \mu\text{A}$
U_{OH} (OUT_x)	Standard versions	min. +2.4V @ $I_{OH} = -6 \text{ mA}$
	OEM version	max. 42V
U_{OL} (OUT_x)	Standard versions	max. +0.45V @ $I_{OL} = 7.8 \text{ mA}$
	OEM version	typ. 0.35V, max. 0.6V
I_O	OEM version	max. 30 mA (see also pageSeite 21)
P_O	OEM version	$U_{OH} \times I_O = \text{max. } 85 \text{ mW}$
U_{EXT}	OEM version	max. 42V
Ground reference		PC ground (GND_PC)

Interrupt input (TTL)Condition: $T_A = 25^{\circ}\text{C}$

Element	Condition	Specification
Number	Pin 48 (EXT_IRQ)	1 x external interrupt interrupt
Level		+5V TTL inputs (see also digital-I/Os)
Ground reference		PC ground (GND_PC)

General

Element	Condition	Specification
PC interface	cPCI models	CompactPCI bus (32 bit, 33 MHz) Rev. 2.2
Power consumption	+5V	typ. 370 mA (without external load)
	+3.3V	typ. 18 mA (without external load)
Temperature range	Operation	0..70 °C
	Storage	-40..100 °C
Humidity	Operation	20%..55% (not condensing)
	Storage	5%..90% (not condensing)
Physical size (without mounting bracket and connectors)	cPCI models	3 HE CompactPCI board
Connectors	cPCI models	78-pin D-Sub female connector (ST1) 25-pin D-Sub female connector (ST2) via additional mounting bracket
Certifications		EMC Directive 2004/108/EG, Emission EN 55022, Noise immunity EN 50082-2, RoHS
Manufacturer warranty		36 months

4.2 Pinouts

4.2.1 78-pin D-Sub female connector (ST1) ADQ-212/215

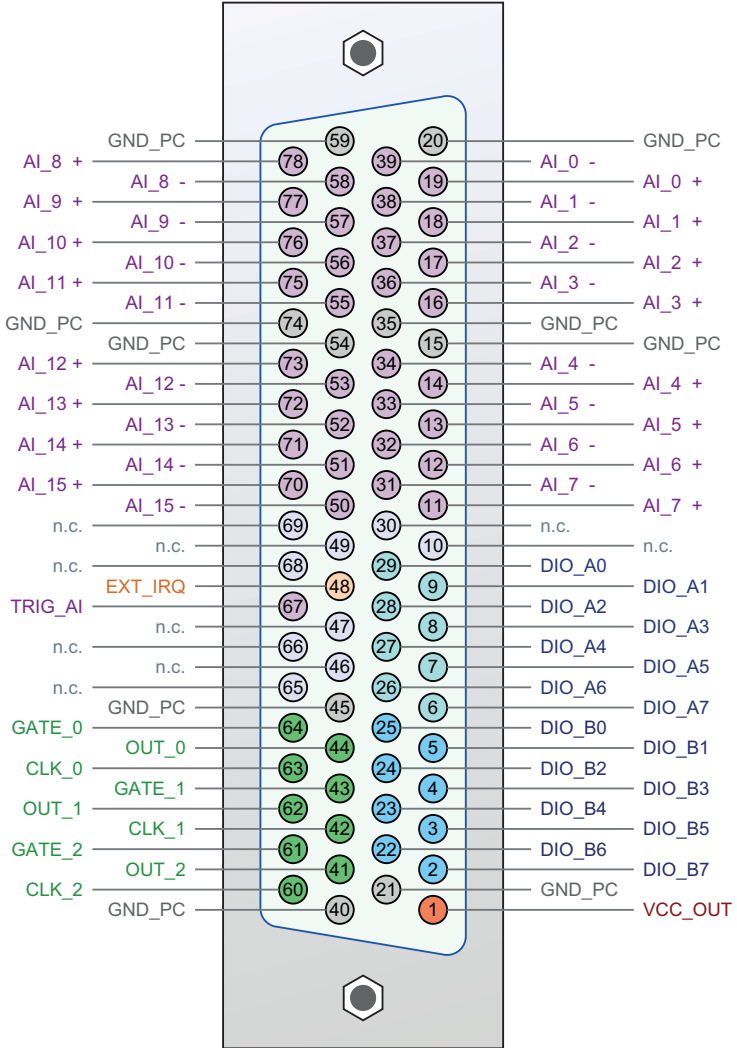


Figure 13: Pinout 78-pin D-Sub female connector (ST1) ADQ-212/215

***Note:** Pin 63 (CLK_0) is not connected on the OEM version.

4.2.2 25-pin D-Sub connector (ST2)

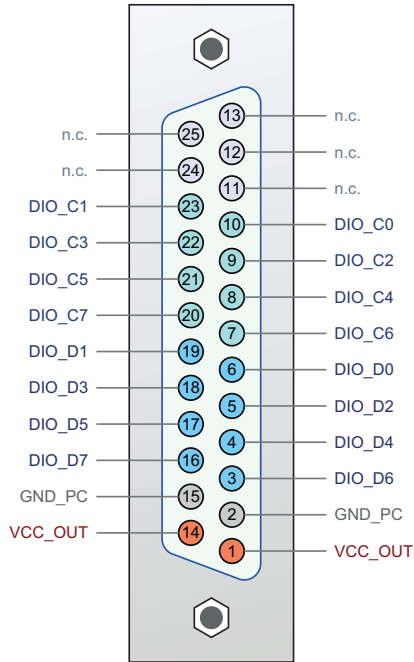
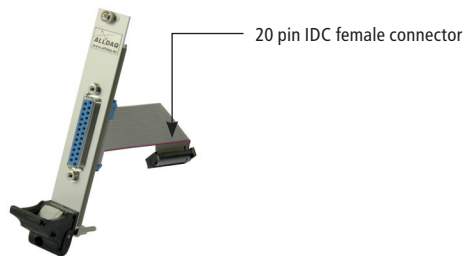


Figure 14: Pinout 25-pin D-Sub female connector (ST2)



CompactPCI bezel with 25-pin D-Sub female connector to 20-pin IDC female connector

Figure 15: Additional mounting bracket/bezel

Refer to page 24 for installation.

Connection of additional mounting bracket/bezel for ST2

For using the TTL digital I/Os (port C and D) an additional mounting bracket/bezel with 25-pin D-Sub female connector to a 20-pin IDC female connector is required (included).

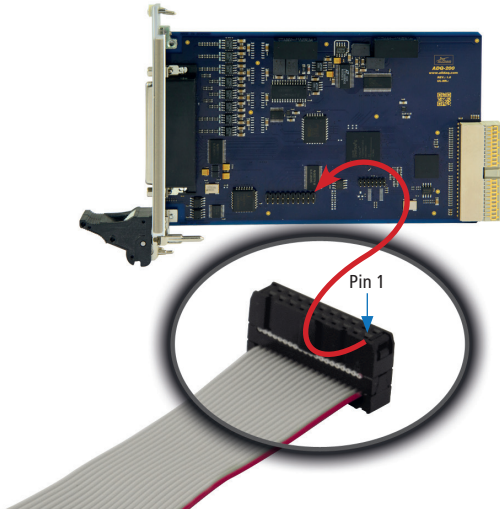


Figure 16: Connection of additional mounting bracket/bezel



Attention: when connecting the IDC female connector make sure to plug pin 1 of the flat ribbon cable (red marked line) to pin 1 of the IDC male connector ST2 as shown above.

4.3 Accessories

ADQ-TB-D25M-HUT (Art.-No. 111749)

25-pin connector block for mounting on DIN rail, 25-pin D-Sub male connector to clamps of type „Phoenix“

ADQ-TB-D78M-HUT (Art.-Nr. 111751)

78-pin connector block for mounting on DIN rail, 78-pin D-Sub male connector to clamps of type „Phoenix“

ADQ-CR-D25M-D25F-1,8m (Art.-No. 111752)

Shielded round cable from 25-pin D-Sub male connector to 25-pin D-Sub female connector, length: 1,8m

ADQ-CR-D78M-D78F-1,5m (Art.-No. 111754)

Shielded round cable from 78-pin D-Sub male connector to 78-pin D-Sub female connector, length: 1,5m

ADQ-AP-D25F-cPCI (Art.-Nor. 111755 - included with ADQ-21x-cPCI)

CompactPCI bezel with 25-pin D-Sub female connector to 20-pin IDC female connector

4.4 Manufacturer and support

ALLNET® and ALLDAQ® are registered trademarks of the ALLNET® GmbH Computersysteme. For questions, problems and product information please contact the manufacturer directly:

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4.5 Important notes

4.5.1 Packaging ordinance

Basically manufacturer and distributors are committed to take care, that sales packaging are withdrawn after use from the end user and applied to a new disposal or to a material recycling as a matter of principle (translated according to §4 sentence 1 of VerpackVO). If you have problems as customer on disposal of packaging and shipping material please write an email to info@allnet.de.

4.5.2 Recycling note and RoHS compliance



Please note, that parts of products of ALLNET® GmbH should be disposed in recycling centers resp. may not be disposed via the household waste (printed circuit boards, power adapters and so on).



ALLNET® products are manufactured in accordance with RoHS (RoHS = Restriction of the use of certain hazardous substances).

4.5.3 CE certification

The ADQ-210 series is CE certified.



This device is compliant to the EU directive: 2004/108/EG regarding the electromagnetic compatibility (EMC) and the cross approval of their conformity. The conformity with the directive as stated above is confirmed by the CE sign on the device.

4.5.4 Warranty

Within the warranty time we eliminate manufacturing and material defects free of charge. The warranty terms valid for your country can be found on the homepage of your distributor. If you have questions or problems applying the warranty you can contact us during our normal opening hours under the following phone number +49 (0)89 894 222 – 474 or by email: support@allda.com.

5. Index

A

Accessories	32
Adjustment	11
ALLDAQ-Manager	10
Analog inputs	14

B

Block diagram	13
---------------------	----

C

Calibration	11
Connectors	
25-pin D-Sub (ST2)	30
78-pin D-Sub (ST1)	29
Counter	20

D

Description	6
Differential inputs	15
Digital I/Os bi-directional	18

E

External interrupt	23
External trigger	16

I

Important notes	33
Initial operation	9
Input voltage range	14
Installation	9
Interrupt external	23
Introduction	5

M

Mounting	6
Mounting bracket	31

O

Oversampling	14
--------------------	----

P

Pinout	
25-pin D-Sub connector (ST2)	30
78-pin D-Sub connector (ST1)	29
Programmierung	
Streaming-Betrieb	19
Programming	
Analog inputs	16
Counter	23
Digital I/Os	19
Interrupt	23

S

Safety instructions	5
Sampling theorem (Nyquist)	14
Scope of delivery	5
Single value mode	16
Software installation	
...under Windows	9
Support	32
System requirements	7

T

Test program	9
Timer-controlled acquisition	16
Trigger A/D section	16

W

Warranty 33

Wiring

Analog inputs 15

Counter 20

Counter (PWM) 22

Digital I/Os. 18

Interrupt external. 23

Trigger external 16



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